深 圳 金 亚 太 科 技 有 限 公 司

Shenzhen Geniatech Co.,Ltd.

SPECIFICATION

MODEL: SOM-3568-SMARC

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CONTENT

Revision History

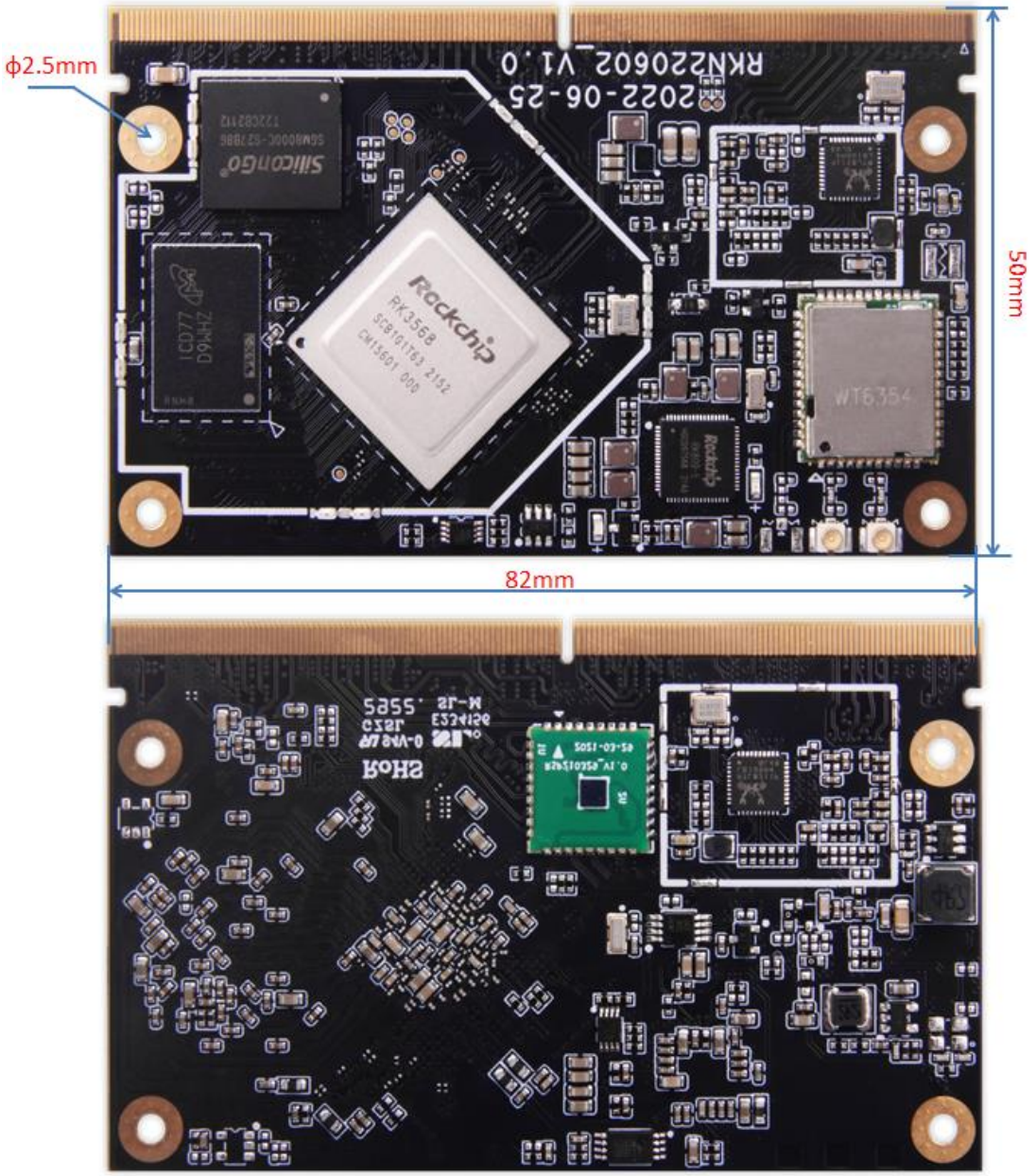
VERSION	DATE	BOARD ID	PAGE	DESCRIPTION	AUTHOR
V1.0	2022/8/10				
V1.1	2022/10/18			Update Pin IO type and level	

1. GENERAL DESCRIPTION

SOM-3568-SMARC is an AI Core board equipped with Rockchip 64-bit processor RK3568 which is configured with dual-core GPU and high-performance NPU, supporting up to 8G RAM. It supports different video input and output interfaces. It is widely used in smart NVR, cloud terminal, industrial automation, Internet of Things application, commercial display and other fields. The following is the detailed specification.

- Adapted with SMARC V2.1 standard
- Supports HDMI interface
- Supports MIPI CSI interface
- Supports LVDS/MIPI DSI interface
- Supports dual Gigabit Ethernet
- Supports 1 lane PCIe 2.1 and 2 lanes PCIe 3.0 interface
- Supports 1 x USB 3.0 host and 2 x USB 2.0 host.
- Supports 1 x USB 3.0 OTG interface.
- Supports 4-bits SDIO 3.0 interface.
- Supports UART/SPI/I2C/GPIO/CAN interface
- Supports Wi-Fi/BT function

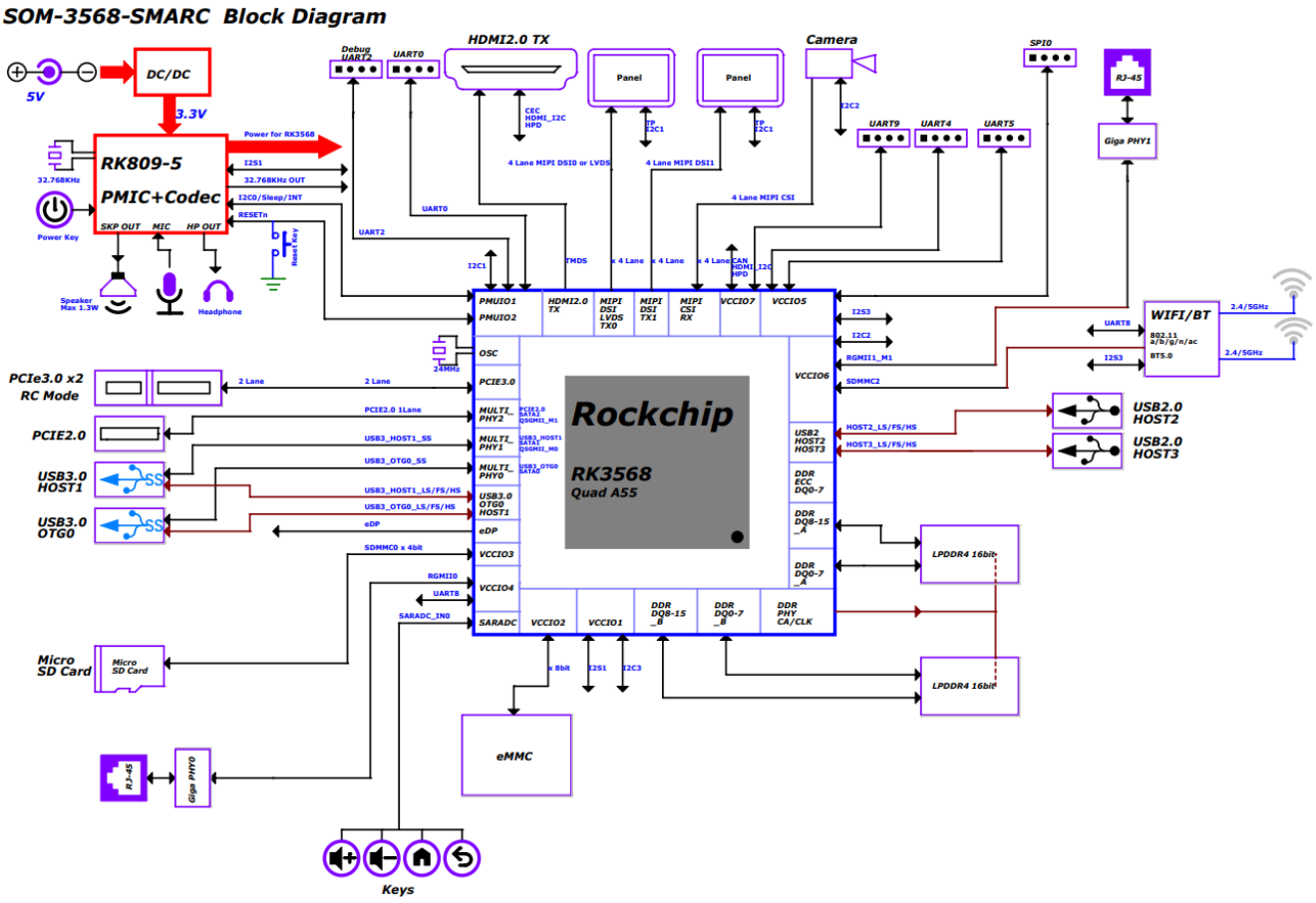
2. PRODUCT APPEARANCE



3. FEATURES

CHIPSET	RockChip RK3568	
MARKET AREA	Global	
OSD LANGUAGE	English/Chinese (multi language OSD)	
Processor	OS	Android 11/Debian
	CPU	Quad-core 64-bit Cortex-A55, 22nm lithography process, frequency up to 2.0GHz
	GPU	ARM G52 2EE Supports OpenGL ES 1.1/2.0/3.2, OpenCL 2.0, Vulkan 1.1 Embedded high-performance 2D acceleration hardware
	NPU	1Tops@INT8, integrated high-performance AI accelerator RKNN NPU Supports one-click switching of Caffe/TensorFlow/TFLite/ONNX/PyTorch/Keras/Darknet
	VPU	Supports 4K 60fps H.265/H.264/VP9 video decoding Supports 1080P 60fps H.265/H.264 video encoding Supports 8M ISP, supports HDR
	RAM	2GB / 4GB / 8GB LPDDR4
	Storage	32GB / 64GB / 128GB eMMC
Interface	Ethernet	*2（Giga ethernet）
	PCIe 2.1	*1(1 lane)
	PCIe 3.0	*1(2 lanes)
	USB2.0	*2
	USB3.0 HOST	*1
	USB3.0 OTG	*1
	MIPI CSI	*1(4 lanes)
	MIPI DSI	*1(DSI0 &DSI1)
	HDMI	*1(HDMI 2.0)
	LVDS	*1(multiplex with DSI1)
	Wi-Fi	*1
	GPIO	*14（or more）
	SDIO	*1
	UART	*6
	SPI	*2
	I2C	*4
	CAN	*1
	I2S	*1
	POWER	5V/2A
Dimensions	82*50 mm	

4. BLOCK DIAGROM



5. SOM MODULE SPECS

5.1 SMARC2.1 specification

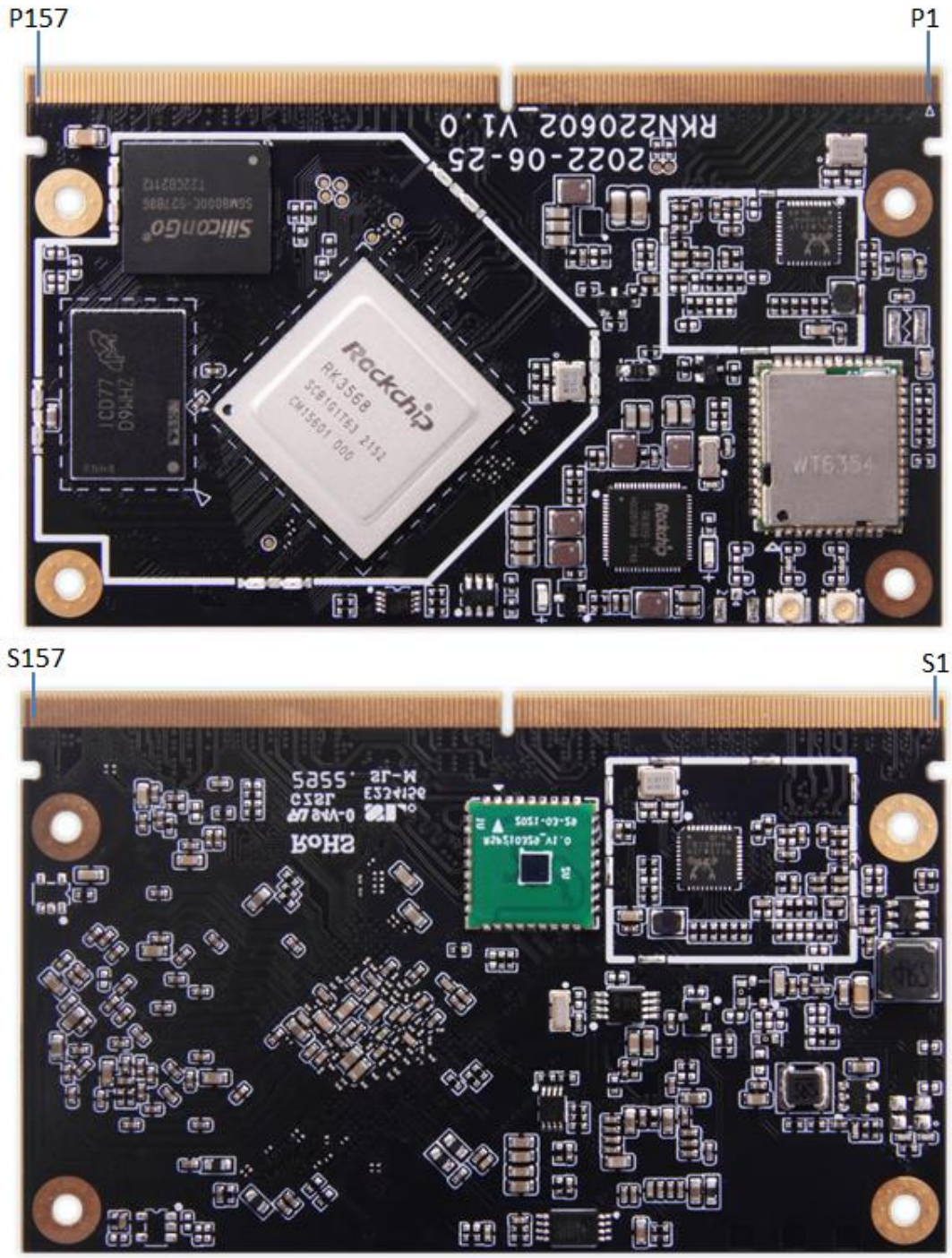
The SMARC (“Smart Mobility Architecture”) is a versatile small form factor computer Module definition targeting applications that require low power, low costs, and high performance. The Modules will typically use ARM SOCs similar or the same as those used in many familiar devices such as tablet computers and smart phones. Alternative low power SOCs and CPUs, such as tablet oriented x86 devices and other RISC CPUs may be used as well. The Module power envelope is typically under 6W although the design up to about 15W is possible.

Two Module sizes are defined: 82mm x 50mm and 82mm x 80mm. The Module PCBs have 314 edge fingers that mate with a low profile 314 pin 0.5mm pitch right angle connector (the

connector is sometimes identified as a 321 pin connector, but 7 pins are lost to the key).

The Modules are used as building blocks for portable and stationary embedded systems. The core CPU and supported circuits (including DRAM, boot flash, power sequencing, CPU power supplies, Gigabit Ethernet and dual channel LVDS display transmitter) are concentrated on the Modules. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, touch controllers, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

5.2 Interface definition



Pin Num	Pin Name	Type	Level	Pin Num	Pin Name	Type	Level
P1	NC			S1	I2C2_SCL_M1	I/O	1.8V
P2	GND			S2	I2C2_SDA_M1	I/O	1.8V
P3	MIPI_CSI_RX_CLK0P	I		S3	GND		
P4	MIPI_CSI_RX_CLK0N	I		S4	VCC3V3_SD		
P5	NC			S5	NC		
P6	NC			S6	CIF_CLKOUT	O	1.8V
P7	MIPI_CSI_RX_D0P	I		S7	NC		
P8	MIPI_CSI_RX_D0N	I		S8	MIPI_CSI_RX_CLK1P	I	
P9	GND			S9	MIPI_CSI_RX_CLK1N	I	
P10	MIPI_CSI_RX_D1P	I		S10	GND		
P11	MIPI_CSI_RX_D1N	I		S11	NC		
P12	GND			S12	NC		
P13	MIPI_CSI_RX_D2P	I		S13	GND		
P14	MIPI_CSI_RX_D2N	I		S14	NC		
P15	GND			S15	NC		
P16	MIPI_CSI_RX_D3P	I		S16	GND		
P17	MIPI_CSI_RX_D3N	I		S17	PHY0_MDI0+	I/O	
P18	GND			S18	PHY0_MDI0-	I/O	
P19	PHY1_MDI3-	I/O		S19	PHY0_LED0/CFG_EXT	O	3.3V
P20	PHY1_MDI3+	I/O		S20	PHY0_MDI1+	I/O	
P21	PHY1_LED0/CFG_EXT	O		S21	PHY0_MDI1-	I/O	
P22	PHY1_LED1/CFG_LDO0	O		S22	PHY0_LED1/CFG_LDO0	O	3.3V
P23	PHY1_MDI2-	I/O		S23	PHY0_MDI2+	I/O	
P24	PHY1_MDI2+	I/O		S24	PHY0_MDI2-	I/O	
P25	PHY1_LED2/CFG_LDO1	O		S25	GND		
P26	PHY1_MDI1-	I/O		S26	PHY0_MDI3+	I/O	
P27	PHY1_MDI1+	I/O		S27	PHY0_MDI3-	I/O	
P28	NC			S28	NC		
P29	PHY1_MDI0-	I/O		S29	NC		
P30	PHY1_MDI0+	I/O		S30	NC		
P31	NC			S31	PHY0_LED2/CFG_LDO1	O	3.3V
P32	GND			S32	NC		
P33	NC			S33	NC		
P34	SDMMC0_CMD	I/O		S34	GND		
P35	SDMMC0_DET_L	I		S35	NC		
P36	SDMMC0_CLK	O		S36	NC		

Pin Num	Pin Name	Type	Level	Pin Num	Pin Name	Type	Level
P37	SDIO_PWR_EN	O	3.3V	S37	USB3_OTG0_VBUSDET	I	USB VBUS
P38	GND			S38	I2S1_MCLK_M0_RK809	O	1.8V
P39	SDMMC0_D0	I/O	1.8V/3.3V	S39	I2S1_LRCK_TX_M0_RK809	I/O	1.8V
P40	SDMMC0_D1	I/O	1.8V/3.3V	S40	I2S1_SDO0_M0_RK809	O	1.8V
P41	SDMMC0_D2	I/O	1.8V/3.3V	S41	I2S1_SDI0_M0/PDM_SDI0_M0_RK809	I	1.8V
P42	SDMMC0_D3	I/O	1.8V/3.3V	S42	I2S1_SCLK_TX_M0_RK809	I/O	1.8V
P43	SPI0_CS0_M1	O	1.8V	S43	NC		
P44	SPI0_CLK_M1	O	1.8V	S44	NC		
P45	SPI0_MISO_M1	I	1.8V	S45	NC		
P46	SPI0_MOSI_M1	O	1.8V	S46	NC		
P47	GND			S47	GND		
P48	NC			S48	I2C3_SCL_M0	I/O	1.8V
P49	NC			S49	I2C3_SDA_M0	I/O	1.8V
P50	GND			S50	NC		
P51	NC			S51	NC		
P52	NC			S52	NC		
P53	GND			S53	NC		
P54	FSPI_CS0n/FLASH_CS0n	O	1.8V	S54	NC		
P55	NC			S55	NC		
P56	FSPI_CLK/FLASH_ALE	O	1.8V	S56	FSPI_D2	O	1.8V
P57	FSPI_D1/FLASH_RDn	I	1.8V	S57	FSPI_D3/FLASH_CS1n	I/O	1.8V
P58	FSPI_D0/FLASH_RDY	O	1.8V	S58	NC		
P59	GND			S59	NC		
P60	USB2_HOST3_DP	I/O	USB	S60	NC		
P61	USB2_HOST3_DM	I/O	USB	S61	GND		
P62	NC			S62	USB3_OTG0_SSTXP	O	
P63	NC			S63	USB3_OTG0_SSTXN	O	
P64	NC			S64	GND		
P65	USB2_HOST2_DP	I/O	USB	S65	USB3_OTG0_SSRXP	I	
P66	USB2_HOST2_DM	I/O	USB	S66	USB3_OTG0_SSRXN	I	
P67	NC			S67	GND		
P68	GND			S68	USB3_OTG0_DP	I/O	USB
P69	USB3_HOST1_DP	I/O	USB	S69	USB3_OTG0_DM	I/O	USB

Pin Num	Pin Name	Type	Level	Pin Num	Pin Name	Type	Level
P70	USB3_HOST1_DM	I/O	USB	S70	GND		
P71	NC			S71	USB3_HOST1_SSTXP	O	USB SS
P72	UART7_TX_M1	O	1.8V	S72	USB3_HOST1_SSTXN	O	USB SS
P73	UART7_RX_M1	I	1.8V	S73	GND		
P74	NC			S74	USB3_HOST1_SSRXP	I	USB SS
P75	PCIE30X2_PERSTn_M1	O	3.3V	S75	USB3_HOST1_SSRXN	I	USB SS
P76	NC			S76	PCIE20_PERSTn_M2	O	3.3V
P77	PCIE20_CLKREQn_M2	IO	3.3V	S77	NC		
P78	PCIE30X2_CLKREQn_M1	IO	3.3V	S78	PCIE20_RXP	I	
P79	GND			S79	PCIE20_RXN	I	
P80	PCIE20_REFCLKP	O		S80	GND		
P81	PCIE20_REFCLKN	O		S81	PCIE20_TXP	O	
P82	GND			S82	PCIE20_TXN	O	
P83	PCIE30_REFCLKP_IN	O		S83	GND		
P84	PCIE30_REFCLKN_IN	O		S84	NC		
P85	GND			S85	NC		
P86	PCIE30_RX0P	I		S86	GND		
P87	PCIE30_RX0N	I		S87	PCIE30_RX1P	I	
P88	GND			S88	PCIE30_RX1P	I	
P89	PCIE30_TX0P	O		S89	GND		
P90	PCIE30_TX0N	O		S90	PCIE30_TX1P	O	
P91	GND			S91	PCIE30_TX1P	O	
P92	HDMI_TX2P_PORT	O		S92	GND		
P93	HDMI_TX2N_PORT	O		S93	NC		
P94	GND			S94	NC		
P95	HDMI_TX1P_PORT	O		S95	NC		
P96	HDMI_TX1N_PORT	O		S96	NC		
P97	GND			S97	NC		
P98	HDMI_TX0P_PORT	O		S98	NC		
P99	HDMI_TX0N_PORT	O		S99	NC		
P100	GND			S100	NC		
P101	HDMI_TXCLKP_PORT	O		S101	GND		
P102	HDMI_TXCLKN_PORT	O		S102	NC		
P103	GND			S103	NC		
P104	HDMI_TX_HPDIN			S104	USB3_OTG0_ID	I	3.3V
P105	HDMITX_SCL	O		S105	NC		

Pin Num	Pin Name	Type	Level	Pin Num	Pin Name	Type	Level
P106	HDMITX _SDA	I/O	1.8V	S106	NC		
P107	HDMITX_CEC_M0	I	1.8V	S107	4G_PWREN_H_GPIO0_C6	O	1.8V
P108	MIPI_CAM0_PDN_L_GPIO3_D5	O	1.8V	S108	MIPI_DSI_TX1_CLKP		
P109	MIPI_CAM1_PDN_L_GPIO3_D3	0	1.8V	S109	MIPI_DSI_TX1_CLKN	O	
P110	MIPI_CAM0_RST_L_GPIO3_D4	O	1.8V	S110	GND		
P111	MIPI_CAM1_RST_L_GPIO3_D2	O	1.8V	S111	MIPI_DSI_TX1_D0P	O	
P112	DVP_PWREN0_H_GPIO0_B0	O	1.8V/ 1.5V	S112	MIPI_DSI_TX1_D0N	O	
P113	PWM3_IR	O	1.8V	S113	NC		
P114	REFCLK_OUT	O	1.8V	S114	MIPI_DSI_TX1_D1P	O	
P115	USB_HOST_PWREN_H_GPIO0_A6	O		S115	MIPI_DSI_TX1_D1N	O	
P116	USB_OTG_PWREN_H_GPIO0_A5	O		S116	LCD1_PWREN_H_GPIO0_C5	O	1.8V
P117	TP_INT_L_GPIO0_B5	I		S117	MIPI_DSI_TX1_D2P	O	
P118	TP_RST_L_GPIO0_B6	O		S118	MIPI_DSI_TX1_D2N	O	
P119	PCIE_PWREN_H_GPIO0_D4	O		S119	GND		
P120	GND			S120	MIPI_DSI_TX1_D3P	O	
P121	NC			S121	MIPI_DSI_TX1_D3N	O	
P122	NC			S122	LCD1_BL_PWM5	O	1.8V
P123	NC			S123	HDMIRX_PWREN_H_GPIO0_D6	O	1.8V
P124	NC			S124	GND		
P125	NC			S125	MIPI_DSI_TX0_D0P/LVDS_TX0_D0P	O	
P126	NC			S126	MIPI_DSI_TX0_D0N/LVDS_TX0_D0N	O	
P127	RESETn	I	1.8V to 5V	S127	LCD_EN_H_GPIO3_C6	O	1.8V
P128	RK809_PWRON	I	1.8V to 5V	S128	MIPI_DSI_TX0_D1P/LVDS_TX0_D1P	O	
P129	UART2_TX_M0_DEBUG	O	1.8V	S129	MIPI_DSI_TX0_D1N/LVDS_TX0_D1N	O	
P130	UART2_RX_M0_DEBUG	I	1.8V	S130	GND		

Pin Num	Pin Name	Type	Level	Pin Num	Pin Name	Type	Level
P131	NC			S131	MIPI_DSI_TX0_D2P/LVDS_TX0_D2P	O	
P132	NC			S132	MIPI_DSI_TX0_D2N/LVDS_TX0_D2N	O	
P133	GND			S133	LCD0_PWREN_H_GPIO0_C7	O	1.8V
P134	UART9_TX_M1	O	1.8V	S134	MIPI_DSI_TX0_CLKP/LVDS_TX0_CLKP	I/O	
P135	UART9_RX_M1	I	1.8V	S135	MIPI_DSI_TX0_CLKN/LVDS_TX0_CLKN	I/O	
P136	UART0_TX	O	1.8V	S136	GND		
P137	UART0_RX	I	1.8V	S137	MIPI_DSI_TX0_D3P/LVDS_TX0_D3P	O	
P138	NC			S138	MIPI_DSI_TX0_D3N/LVDS_TX0_D3N	O	
P139	NC			S139	I2C1_SCL_TP	I/O	1.8V
P140	UART5_TX_M1	O	1.8V	S140	I2C1_SDA_TP	I/O	1.8V
P141	UART5_RX_M1	I	1.8V	S141	LCD0_BL_PWM4	O	1.8V
P142	GND			S142	HDMIRX_DET_L_GPIO3_D0	I/O	1.8V
P143	UART4_TX_M1/GPIO3_B2	O	1.8V	S143	GND		
P144	UART4_RX_M1/GPIO3_B1	I	1.8V	S144	NC		
P145	CAN1_TX_M1	O	1.8V	S145	NC		
P146	CAN1_RX_M1	I	1.8V	S146	PCIE30X2_WAKEn_M1	I	3.3V
P147	VCC5V0_SYS	Analog	3.0V ~5.25V	S147	VCC_RTC_Backup	Analog	3.0V ~5.25V
P148	VCC5V0_SYS	Analog	3.0V ~5.25V	S148	NC		
P149	VCC5V0_SYS	Analog	3.0V ~5.25V	S149	PMIC_SLEEP_H	I	1.8V~5V
P150	VCC5V0_SYS	Analog	3.0V ~5.25V	S150	NC		
P151	VCC5V0_SYS	Analog	3.0V ~5.25V	S151	NC		
P152	VCC5V0_SYS	Analog	3.0V ~5.25V	S152	NC		
P153	VCC5V0_SYS	Analog	3.0V ~5.25V	S153	NC		

Pin Num	Pin Name	Type	Level	Pin Num	Pin Name	Type	Level
P154	VCC5V0_SYS	Analog	3.0V ~5.25V	S154	EXT_EN	O	1.8V
P155	VCC5V0_SYS	Analog	3.0V ~5.25V	S155	SARADC_VIN0_KEY/ RECOVERY	I	1.8V
P156	VCC5V0_SYS	Analog	3.0V ~5.25V	S156	NC		
				S157	NC		
				S158	GND		

6. MULTIMEDIA

Video

- Video Decoder
  - H.265 HEVC/MVC Main10 Profile yuv420@L5.1 up to 4096x2304@60fps
  - H.264 AVC/MVC Main10 Profile yuv400/yuv420/yuv422/@L5.1 up to 4096x2304@60fps
  - VP9 Profile0/2 yuv420@L5.1 up to 4096x2304@60fps
  - VP8 verision2, up to 1920x1088@60fps
  - VC1 Simple Profile@low, medium, high levels, Main Profile@low, medium, high levels, Advanced Profile@level0~3, up to 1920x1088@60fps
  - MPEG-4 Simple Profile@L0~6, Advanced Simple Profile@L0~5, up to 1920x1088@60fps
  - PEG-2 Main Profile, low, medium and high levels, up to 1920x1088@60fps
  - MPEG-1 Main Profile, low, medium and high levels, up to 1920x1088@60fps
  - H.263 Profile0, levels 10-70, up to 720x576@60fps
- Video Encoder
  - H.264/AVC BP/MP/HP@level4.2, up to 1920x1080@60fps
  - H.265/HEVC MP@level4.1, up to 1920x1080@60fps (4096x4096@10fps with TILE)
  - Support YUV/RGB video source with rotation and mirror

JPEG CODEC

- JPEG decoder
  - JPEG Baseline interleaved, max resolution up to 8176x8176, performance up to 76 million pixels per second
- JPEG encoder
  - Baseline Non-progressive
  - up to 90 million pixels per second

Display System

Graphics Engine

- 3D Graphics Engine:
  - Mali-G52 1-Core-2EE
  - Support OpenGL ES 1.1, 2.0, and 3.2
  - Support Vulkan 1.0 and 1.1
  - Support OpenCL 2.0 Full Profile
  - Support 1600Mpix/s fill rate when 800MHz clock frequency
  - Support 38.4GLOPs when 800MHz clock frequency
- 2D Graphics Engine:

  Data format

- Support input of ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422/YUYV；
- Support input of YUV422SP10bit/YUV420SP10bit(YUV-8bits out)
- Supports output of ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422/YUYV；
- Pixel Format conversion, BT.601/BT.709
- Dither operation, Y dither update;
- Max resolution: 8192x8192 source, 4096x4096 destination

Display interface

- Display interface
  - Supports RGB Parallel Display interface
  - Supports BT656/BT1120 interface
  - Supports MIPI_DSI interface ν Support LVDS interface
  - Supports HDMI interface
  - Supports eDP interface
  - Supports EBC inteface
  - Supports three simultaneous displays in the following interfaces
    - ◆RGB/BT1120
    - ◆BT656
    - ◆MIPI_DSI_TX
    - ◆LVDS
    - ◆HDMI
    - ◆eDP
- MIPI DSI TX interface
  - Compatible with MIPI Alliance Interface specification v1.2
  - Supports 2 channel DSI
  - Supports 4 data lanes per channel
  - Supports 2.5Gbps maximum data rate per lane
  - Up to 1920x1080@60Hz display output for single MIPI mode and 2560*1440@60Hz for dual-MIPI mode
  - Supports RGB(up to 8bit) format
- LVDS interface
  - Compliant with the TIA/EIA-644-A LVDS specification
  - Supports RGB888 and RGB666 input for LVDS interface
  - Supports VESA/JEIDA LVDS data format transfer
- HDMI TX interface
  - Single Physical Layer PHY with support for HDMI1.4 and HDMI2.0 operation
  - For HDMI operation, support for the following:
    - ◆ Up to 10 bits Deep Color modes
    - ◆ Up to 1080p@120Hz and 4096x2304@60Hz
    - ◆ 3-D video formats
  - Supports RGB/YUV(up to 10bit) format

- Supports HDCP1.4/2.2

- eDP interface
  - Supports 1 eDP 1.3 interface
  - Up to 4 physical lanes of 2.7Gbps/lane
  - Supports Panel Self Refresh(PSR)
  - Supports up to 2560x1600@60Hz
  - Supports RGB(up to 10bit) format

7. PRECAUTIONS FOR USE

1.Relative humidity: ≤90% .

2.CPU Operation temperature: Commercial field：0~ 75℃； Industrial field: -20~85℃

3.Do not squeeze, distort or disassemble the PC.

4.Keep the Board away from static electricity .

5.Keep the Board away from water and other liquid.

6.Don’t use long connect wires which may affect performance and image quality.