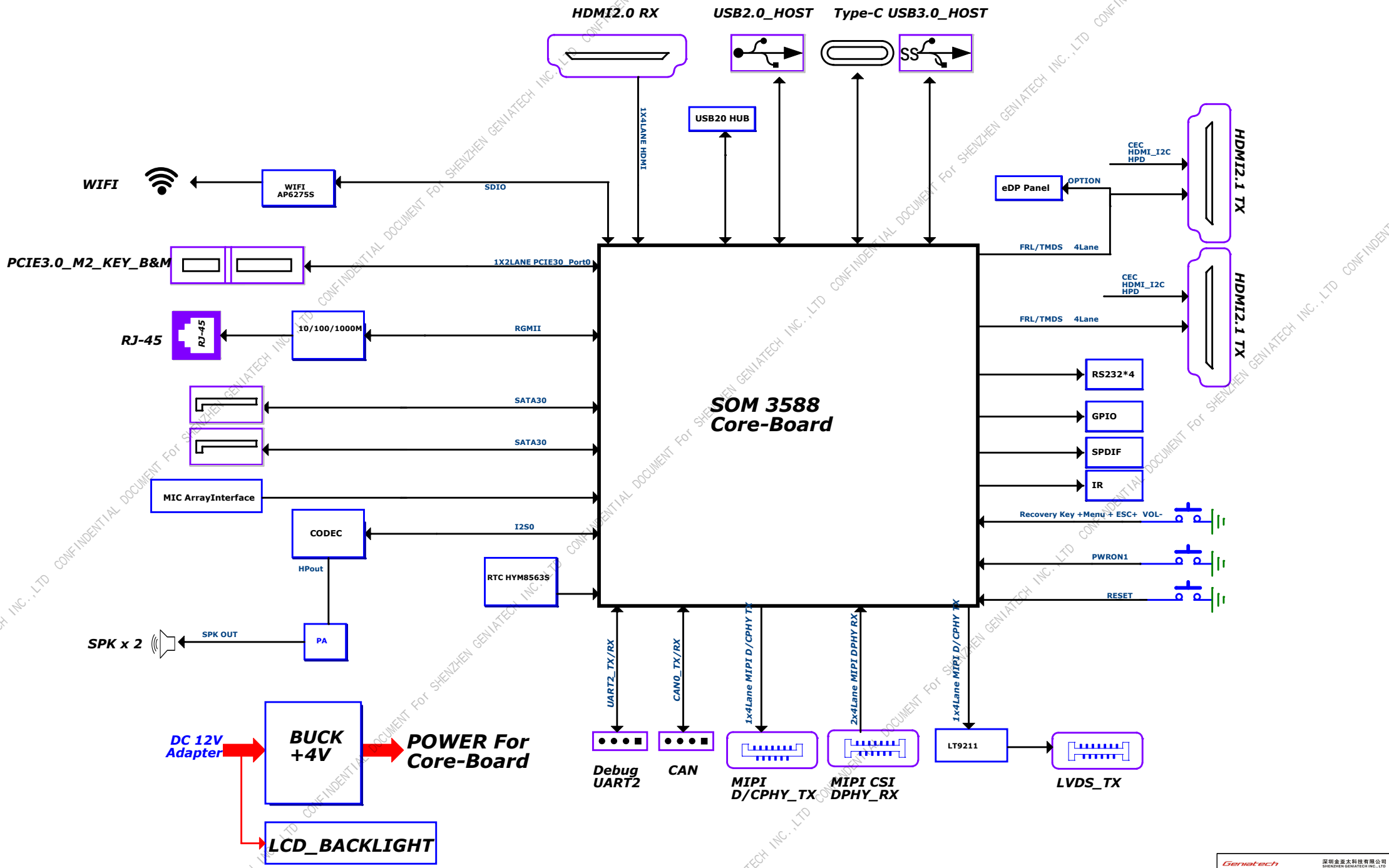
Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2022-05-26	Linta	1:Revision preliminary version	
V1.01	2022-10-28	Linta	1、接口端网络PCIE_5G_WAKE_ON_WAN#与MIPI_CAM3_CLKOUT对调位置 2、U3101 U3103 U2901 U2904 U2906 U2908更改为：RS0102 3、网口封装定义修改 4、LT9211 的I2C网络修改 5、更换RTC电路： HYM8563S 6、更换电源输入DCDC :APW8713A 7、增加MIPI屏接口及对应背光电路：WD101HKM40AB 8、更换摄像头接口：ZH13850-ZH-001 9、增加WIFI模块：AP6275S 10、增加CAN接口：4PIN_3_81MM 11、增加跳线帽来切换HDMI OUT和eDP接口 12、GPIO接口更换为2*12PIN	
V1.02	2023-02-25	Linta	1、增加4P接口（Power按键和LED指示） 2、调整IR位置 3、修正WIFI PIN定义，增加外部电感 4、修改网口接地	
V1.1	2024-04-09	Linta	1、优化RTC功耗大问题 ，增加预留I2C0_M2 2、修改J3002的I2C网络，改为I2C3_M0 3、UART1_M2改为UART2_M1 4、修改为UART0_M2电平 5、修改为SPI_M2电平 6、HDMI增加共模电感	

Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	CBD-3588				
File:	02.Revision History				
Date:	Thursday, April 11, 2024			Rev:	V1.1
Designed by:	Linta	Reviewed by:	cjx	Sheet:	1 of 31



Geniatech	深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD
Project:	CBD-3588
File:	03.Block Diagram
Date:	Thursday, April 11, 2024
Rev:	V1.1
Designed by:	Linta
Reviewed by:	cjx
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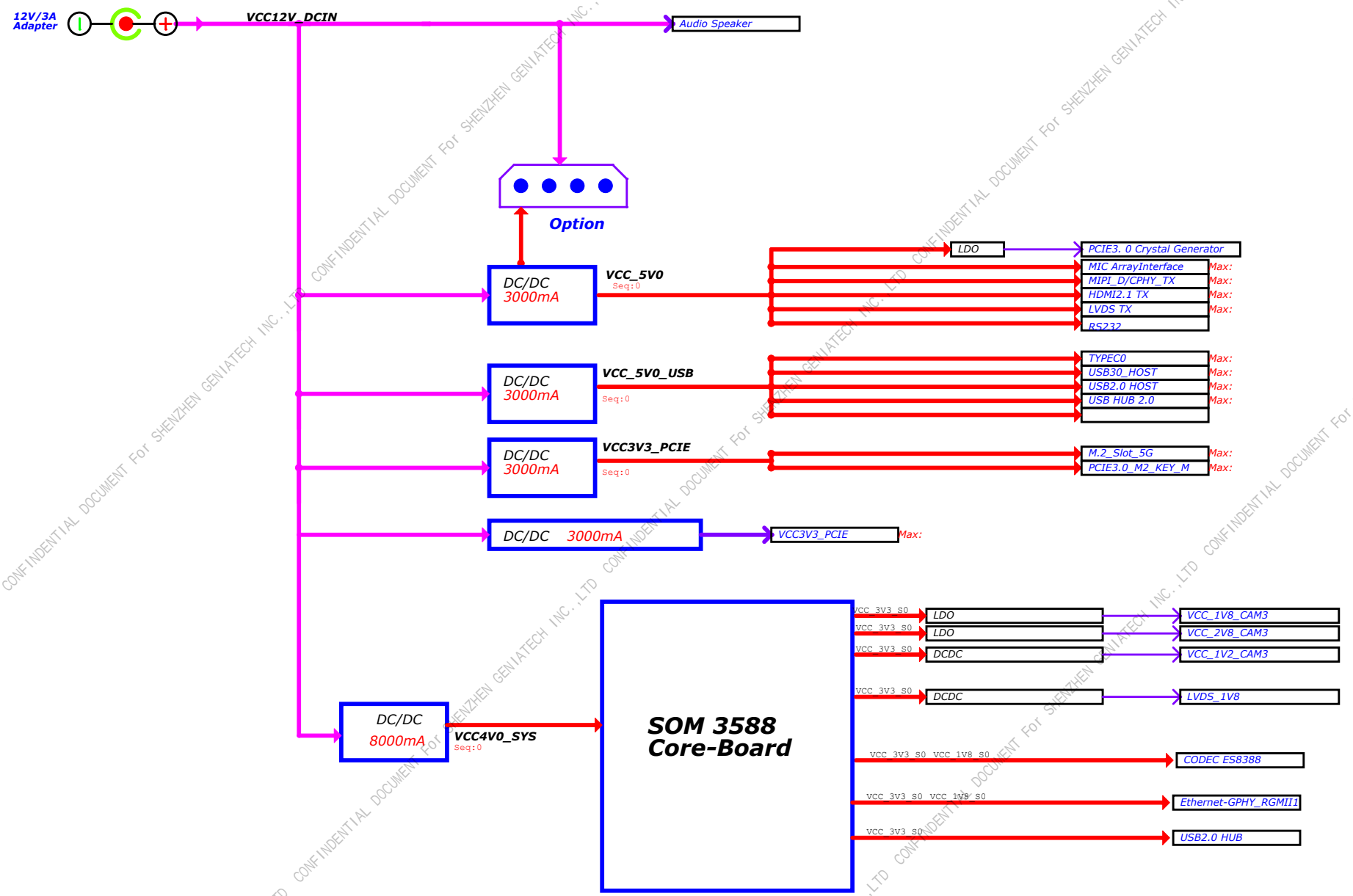
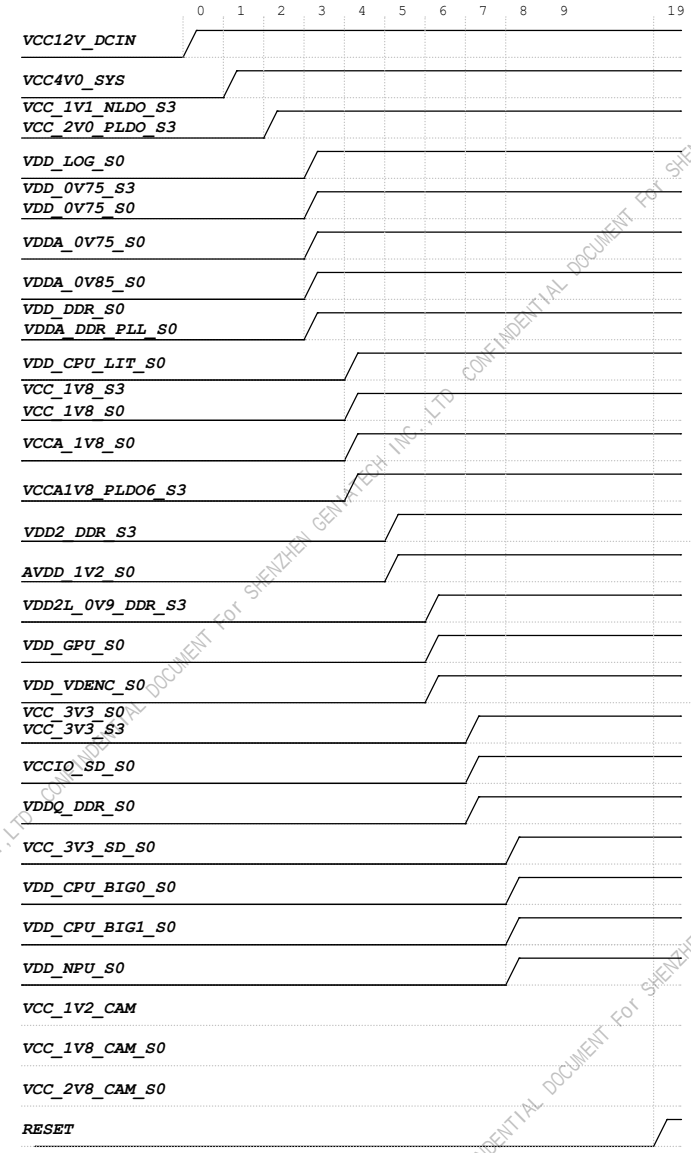
Power Tree



Geniatech	深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD
Project:	CBD-3588
File:	04.Power Tree
Date:	Thursday, April 11, 2024
Rev:	V1.1
Designed by:	Linta
Reviewed by:	cjx
Sheet:	3 of 31

Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC4V0_SYS	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO	RK806-1_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_3V3_S3	EXT_BUCK	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	IO Operating Voltage
PMUIO1	Pin N28	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin R27 Pin P28	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8_S3	1.8V
EMMCIO	Pin V26	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin G20	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AA7 Pin Y7	1.8V or 3.3V	VCCIO2_1V8 VCCIO2	VCC_1V8_S0 VCC_IO_SD	1.8V/3.3V
VCCIO3	Pin Y26	1.8V Only	VCCIO3_1V8	VCC_1V8_S0	1.8V
VCCIO4	Pin H20 Pin H21	1.8V or 3.3V	VCCIO4_1V8 VCCIO4	VCC_1V8_S0 VCC_1V8_S0	1.8V
VCCIO5	Pin W25 Pin W26	1.8V or 3.3V	VCCIO5_1V8 VCCIO5	VCC_1V8_S0 VCC_3V3_S0	3.3V
VCCIO6	Pin AC25 Pin AC26	1.8V or 3.3V	VCCIO6_1V8 VCCIO6	VCC_1V8_S0 VCC_3V3_S0	3.3V

Geniatech	深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD
Project:	CBD-3588
File:	05.System Power Sequence
Date:	Thursday, April 11, 2024
Rev:	V1.1
Designed by:	Linta
Reviewed by:	cjx
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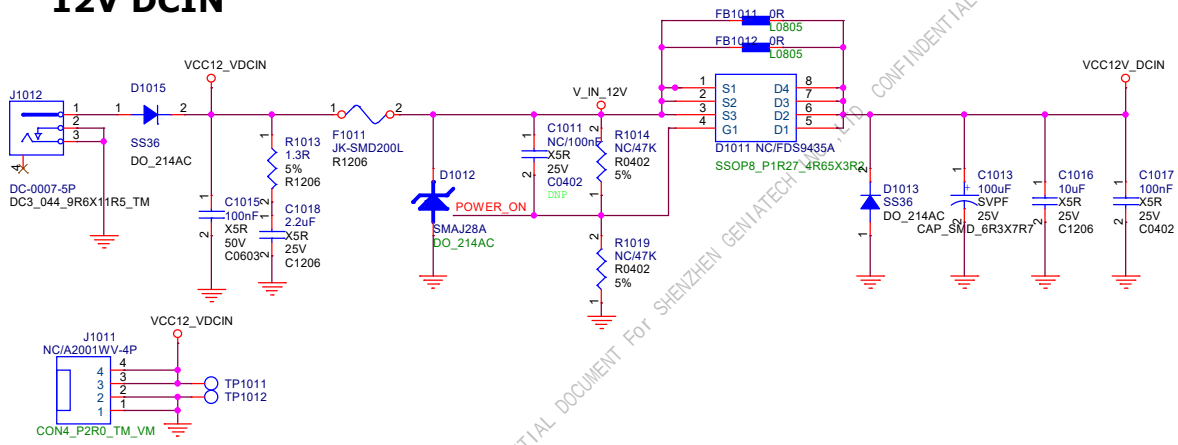
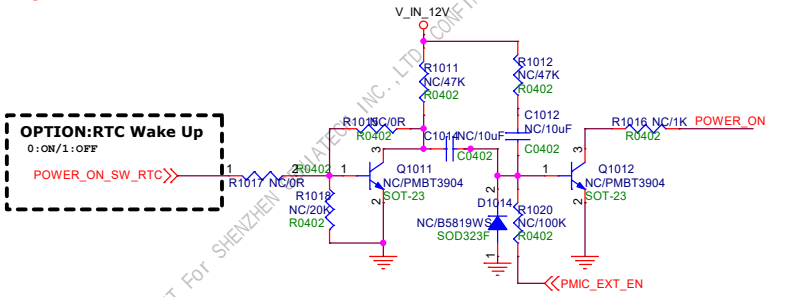
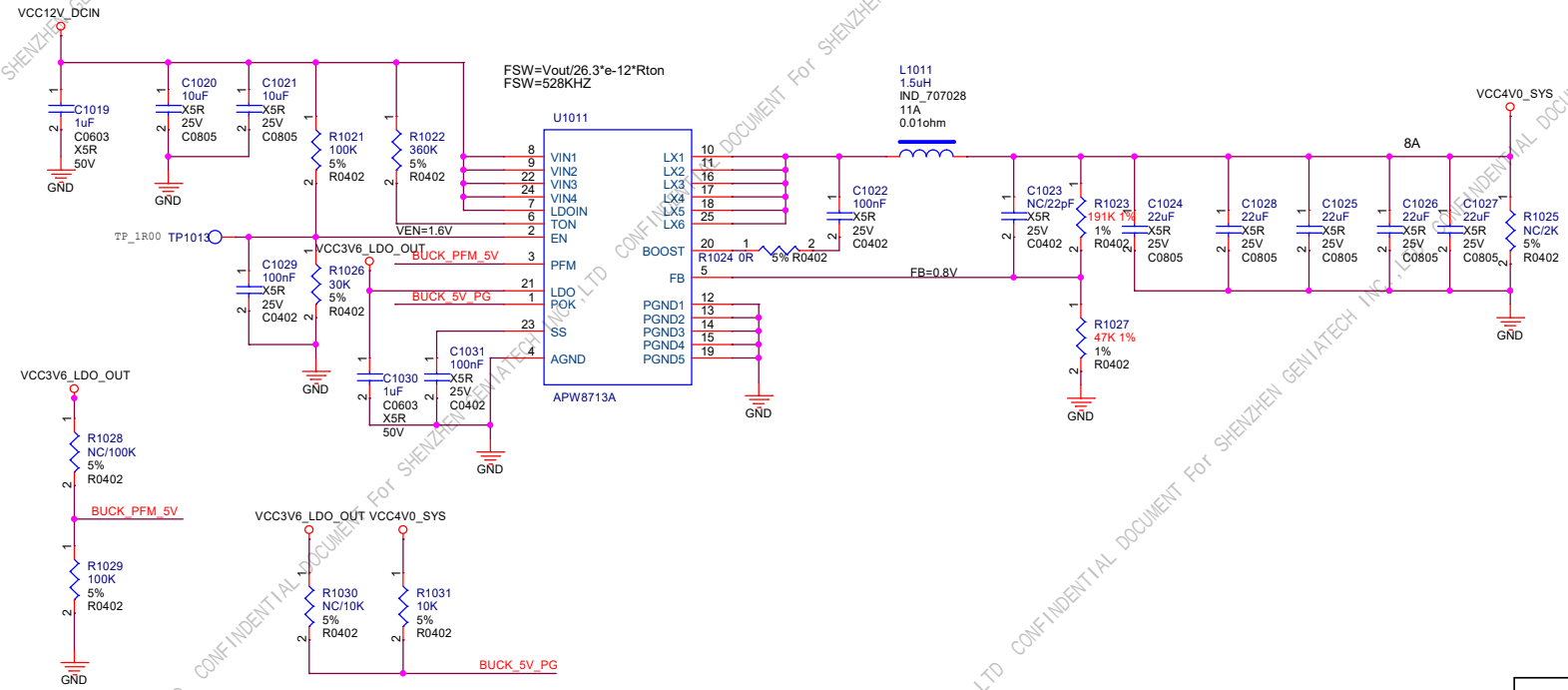
12V DCIN



Option



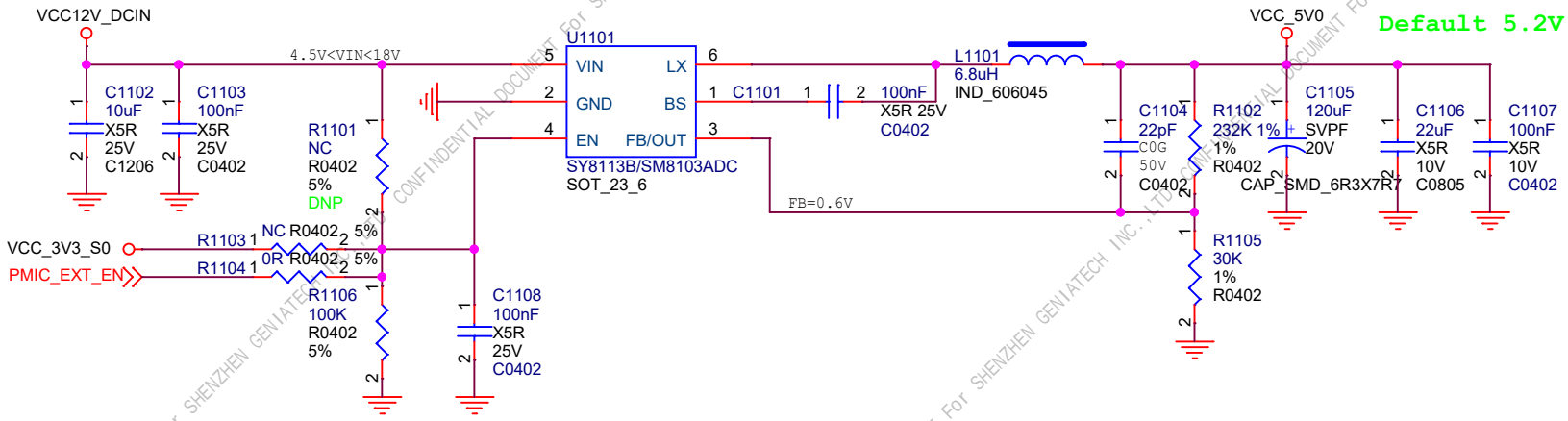
VCC4V0_SYS



Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	CBD-3588				
File:	10.Power_DC IN/VCC4V0_SYS				
Date:	Friday, April 12, 2024			Rev:	V1.1
Designed by:	Linta	Reviewed by:	cjx	Sheet:	5 of 31

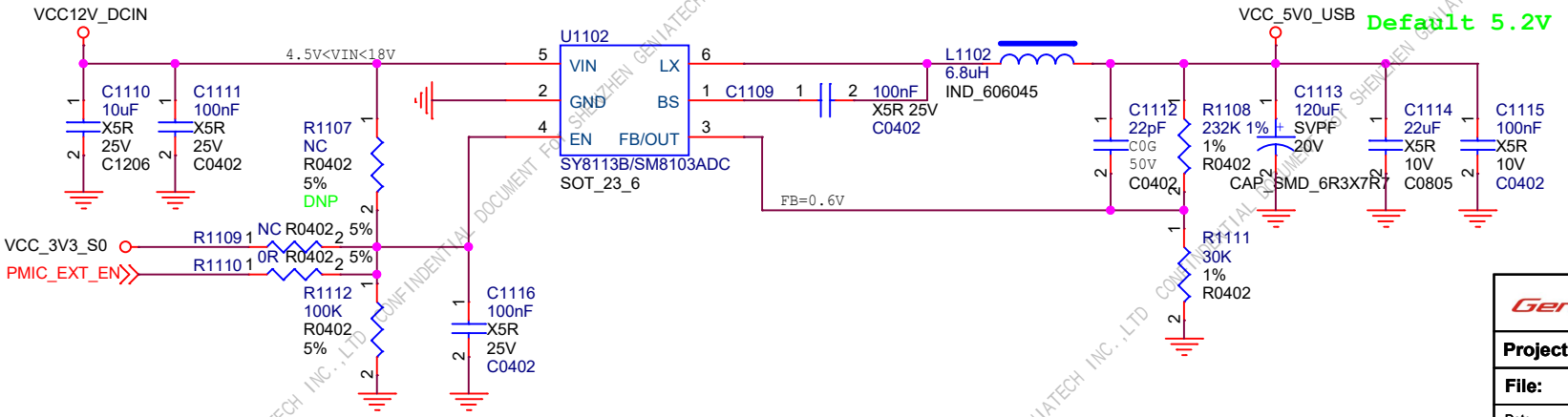
VCC5V0_SYS

Output Support 5V/3A



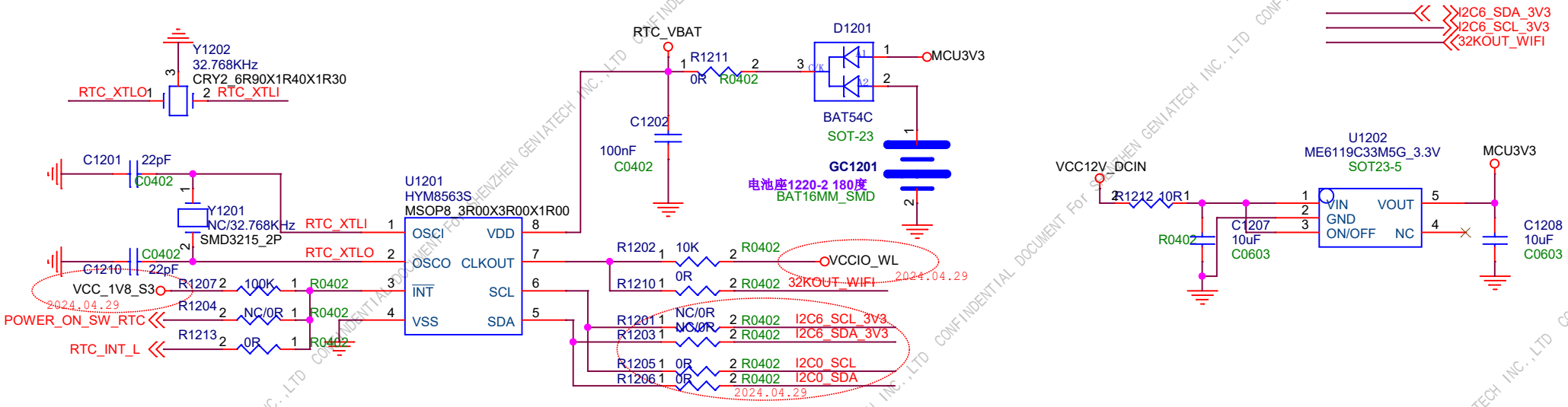
VCC5V0_SYS

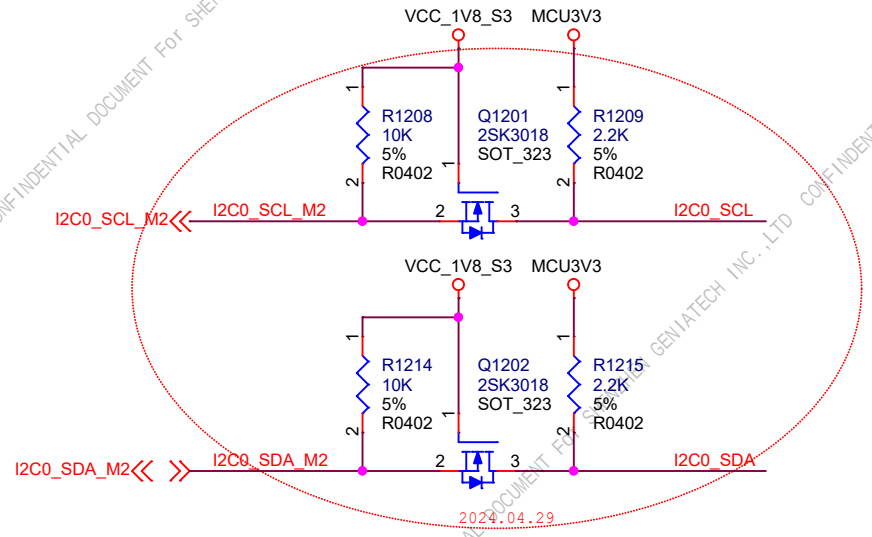
Output Support 5V/3A



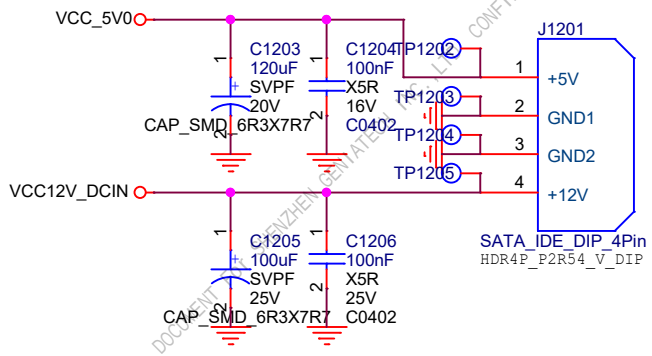
Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	CBD-3588				
File:	11.Power_Ext VCC_5V0				
Date:	Thursday, April 11, 2024			Rev:	V1.1
Designed by:	Linta	Reviewed by:	cjx	Sheet:	6 of 31

RTC



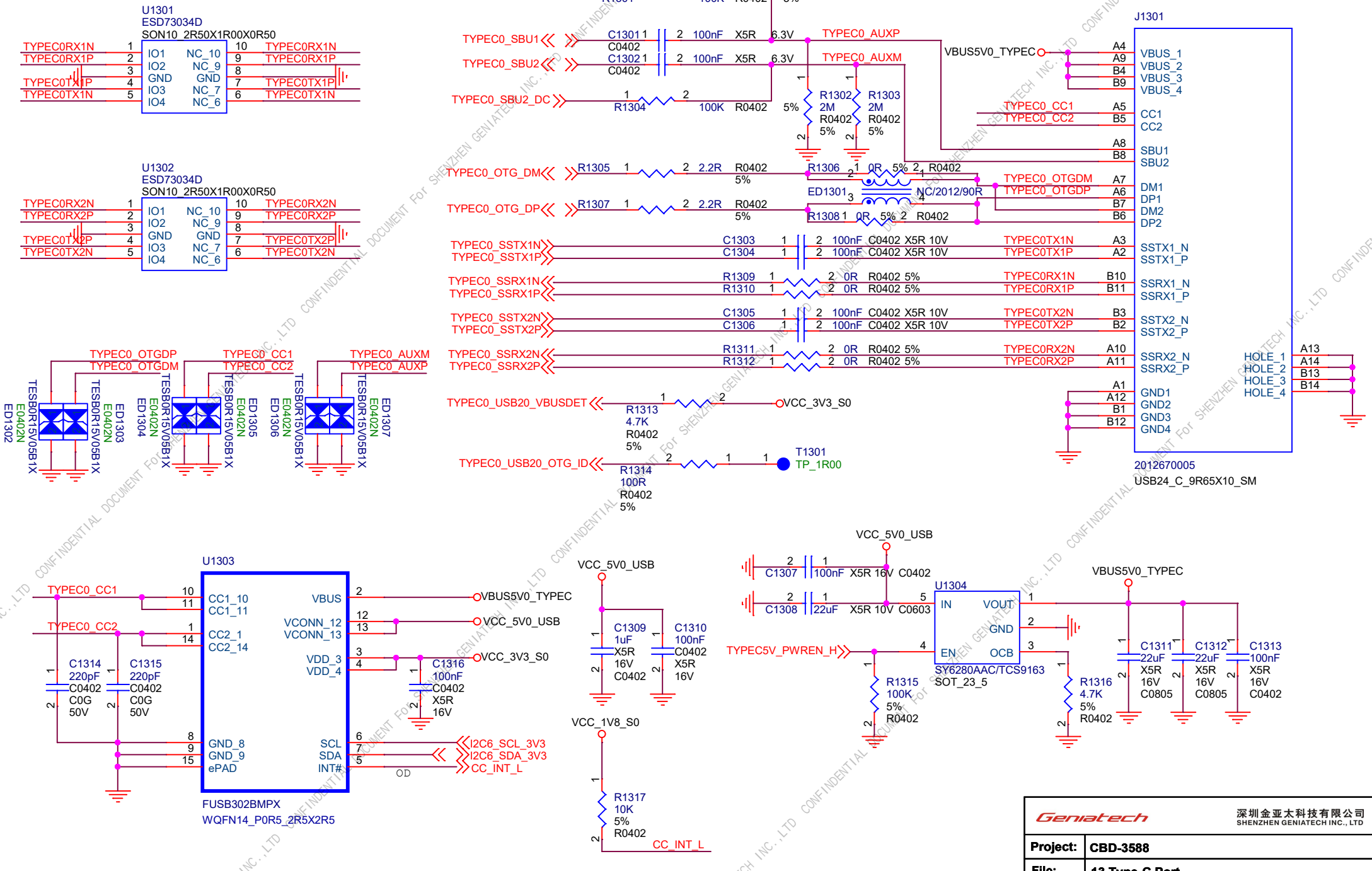


SATA_POWER



Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	CBD-3588				
File:	12.RTC WDT/SATA POWER				
Date:	Friday, April 12, 2024			Rev:	V1.1
Designed by:	Linta	Reviewed by:	cjx	Sheet:	7 of 31

Type-C PORT



Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	CBD-3588				
File:	13.Type-C Port				
Date:	Friday, April 12, 2024			Rev:	V1.1
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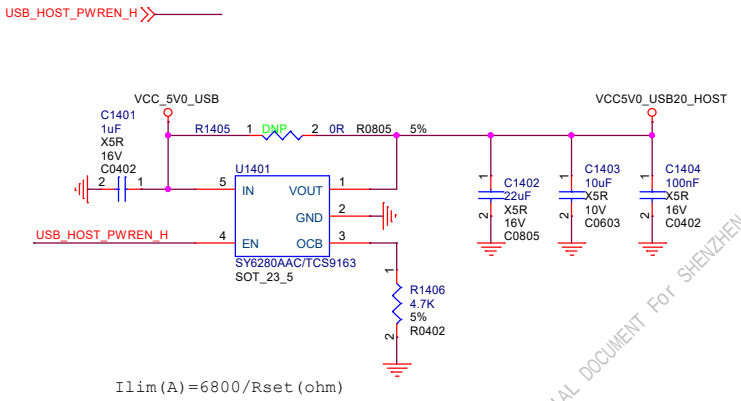
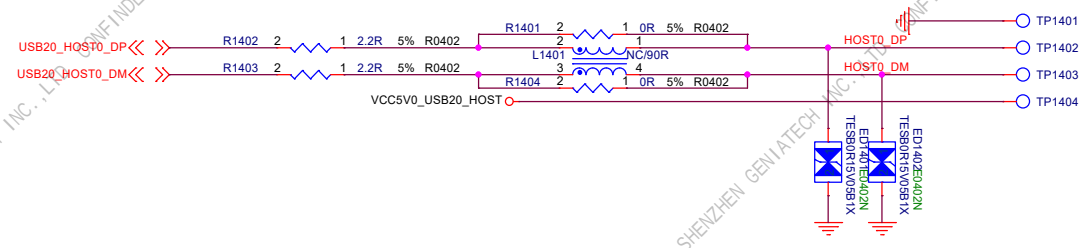
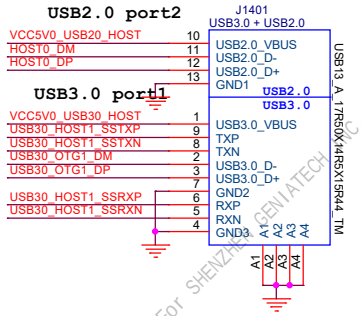
USB2.0 HOST PORT



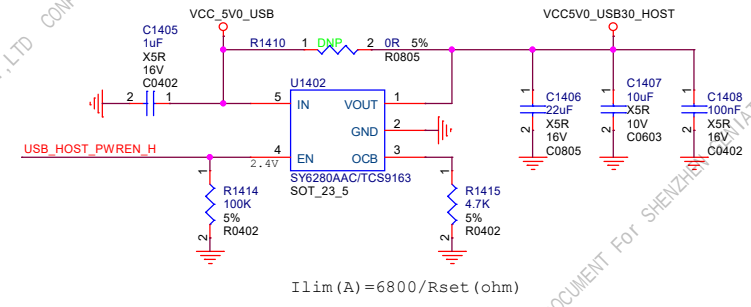


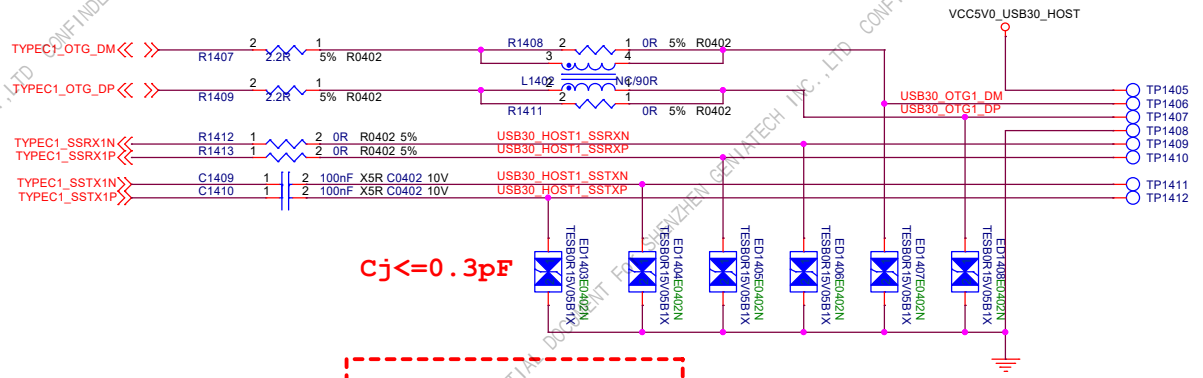
USB2.0+USB3.0 Port

双层USB座，下层USB3.0，上层USB2.0



USB3.0 HOST PORT





Cj<=0.3pF

Note:
The Cj of ESD must <=0.3pf

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Project:	CBD-3588				
File:	14.USB20/USB30 Port				
Date:	Friday, April 12, 2024			Rev:	V1.1
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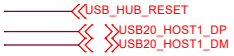
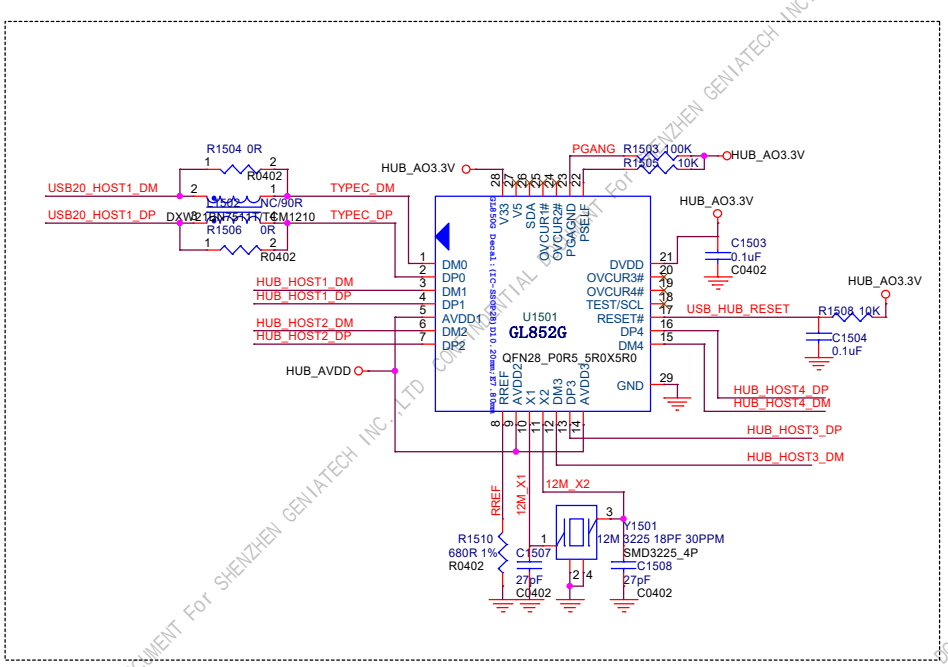
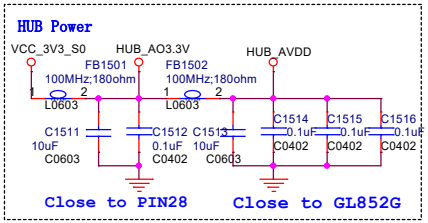
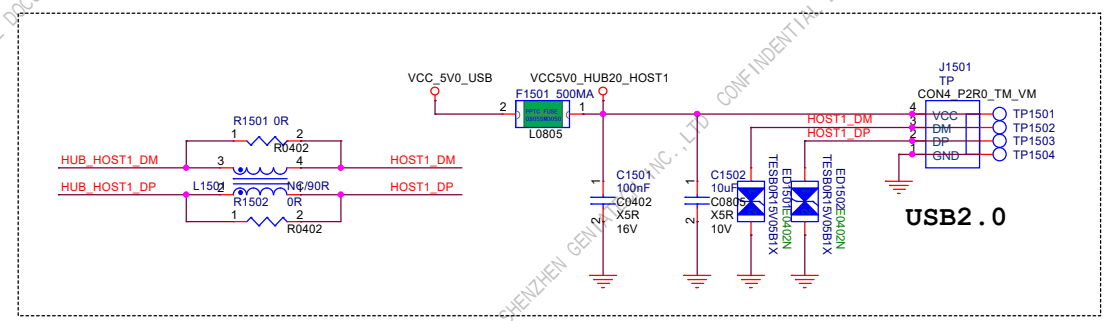
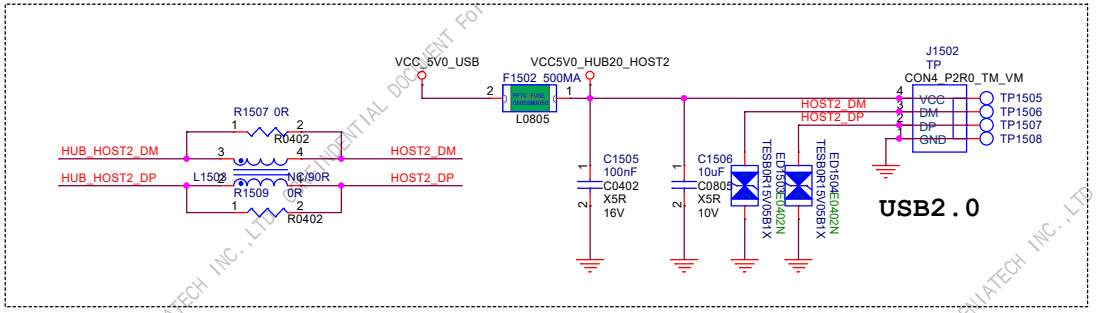
USB2.0 HUB

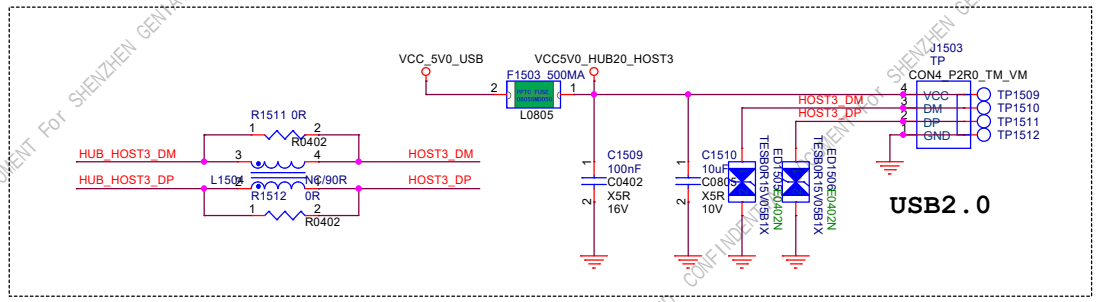


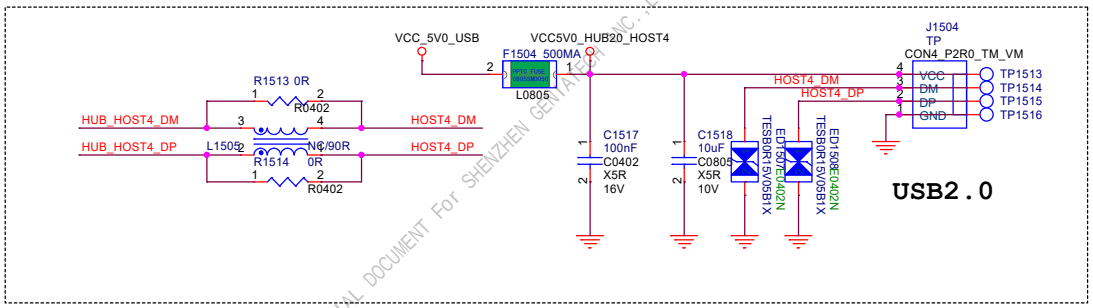






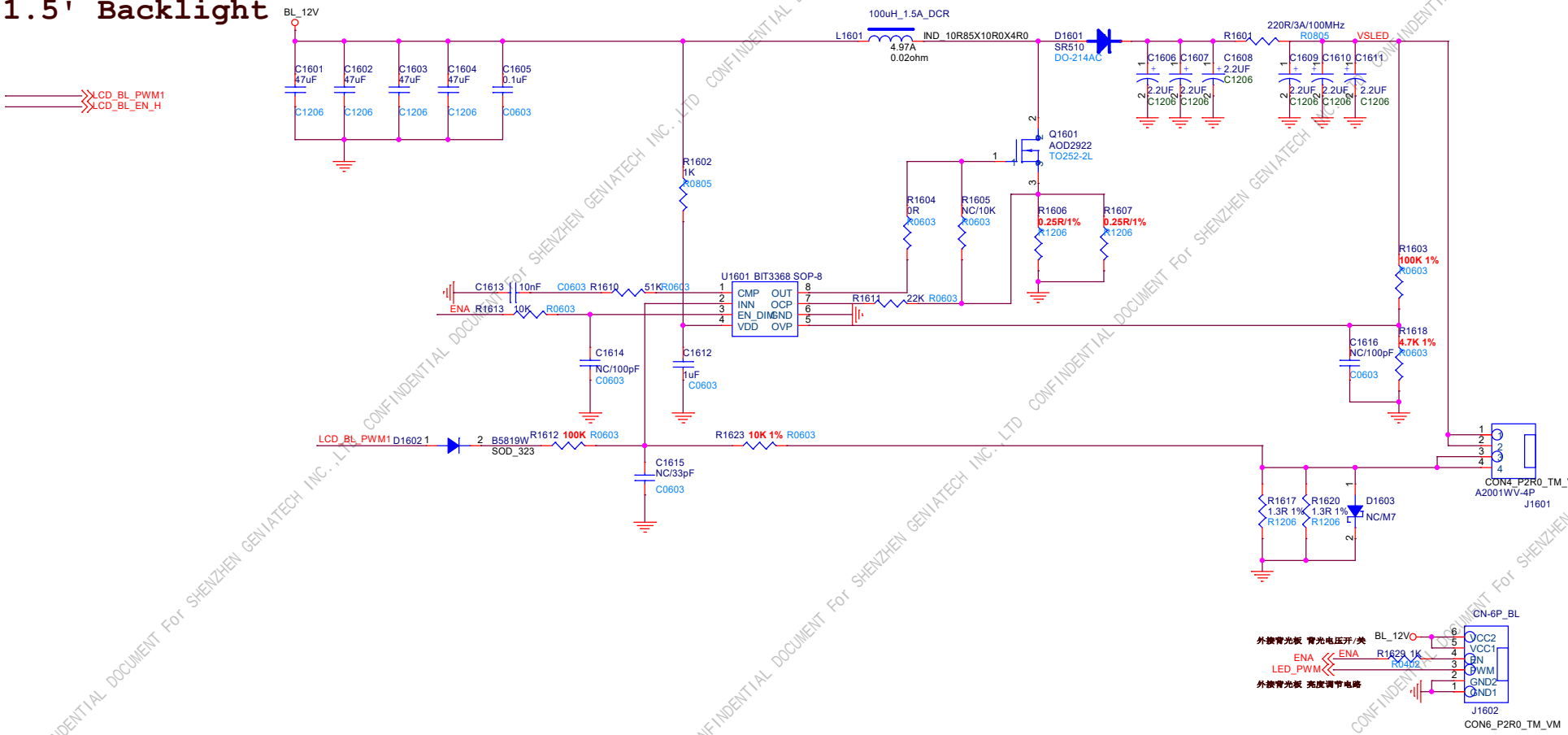




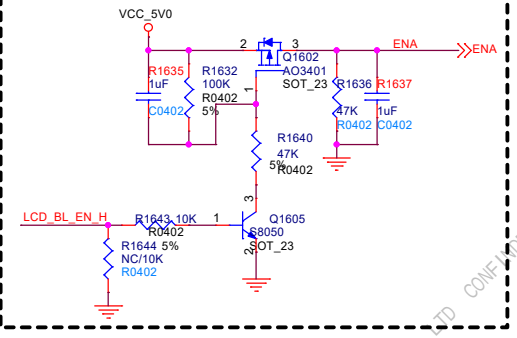


Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	CBD-3588				
File:	15.USB HUB GL85x				
Date:	Friday, April 12, 2024			Rev:	V1.1
Designed by:	Linta	Reviewed by:	cjx	Sheet:	10 of 31

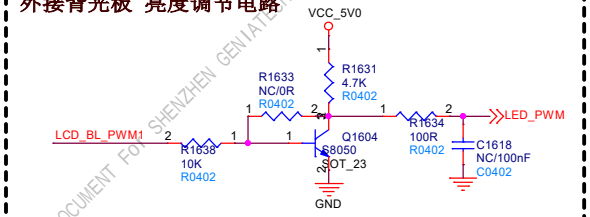
21.5' Backlight



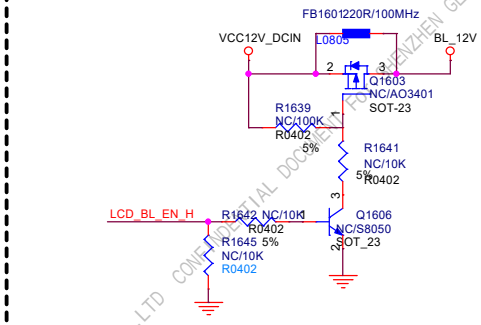
控制背光电压 开/关



外接背光板 亮度调节电路



外接背光电压供电 开/关



Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	CBD-3588				
File:	16.LCD_BACKLIGHT				
Date:	Friday, April 12, 2024			Rev:	V1.1
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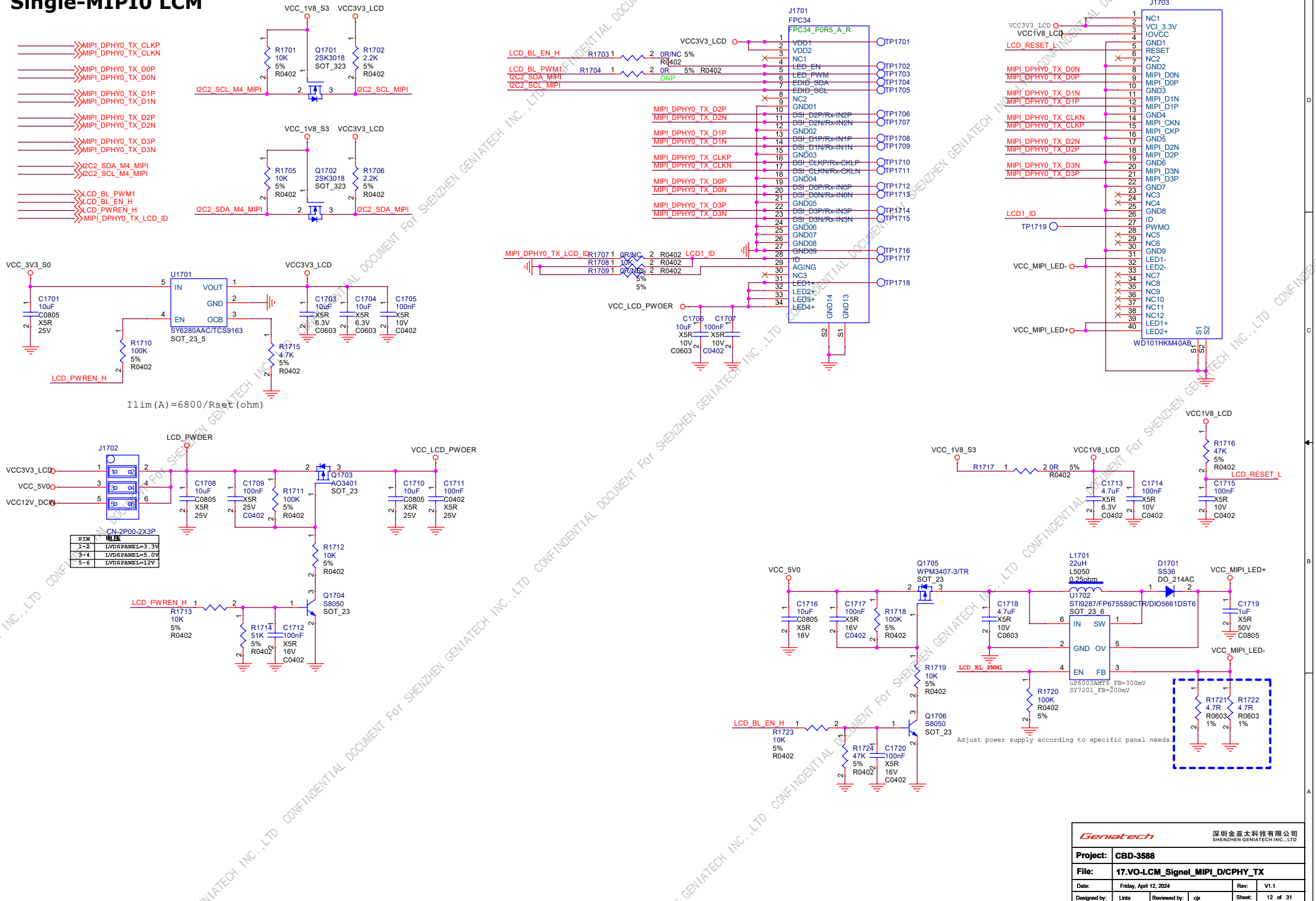
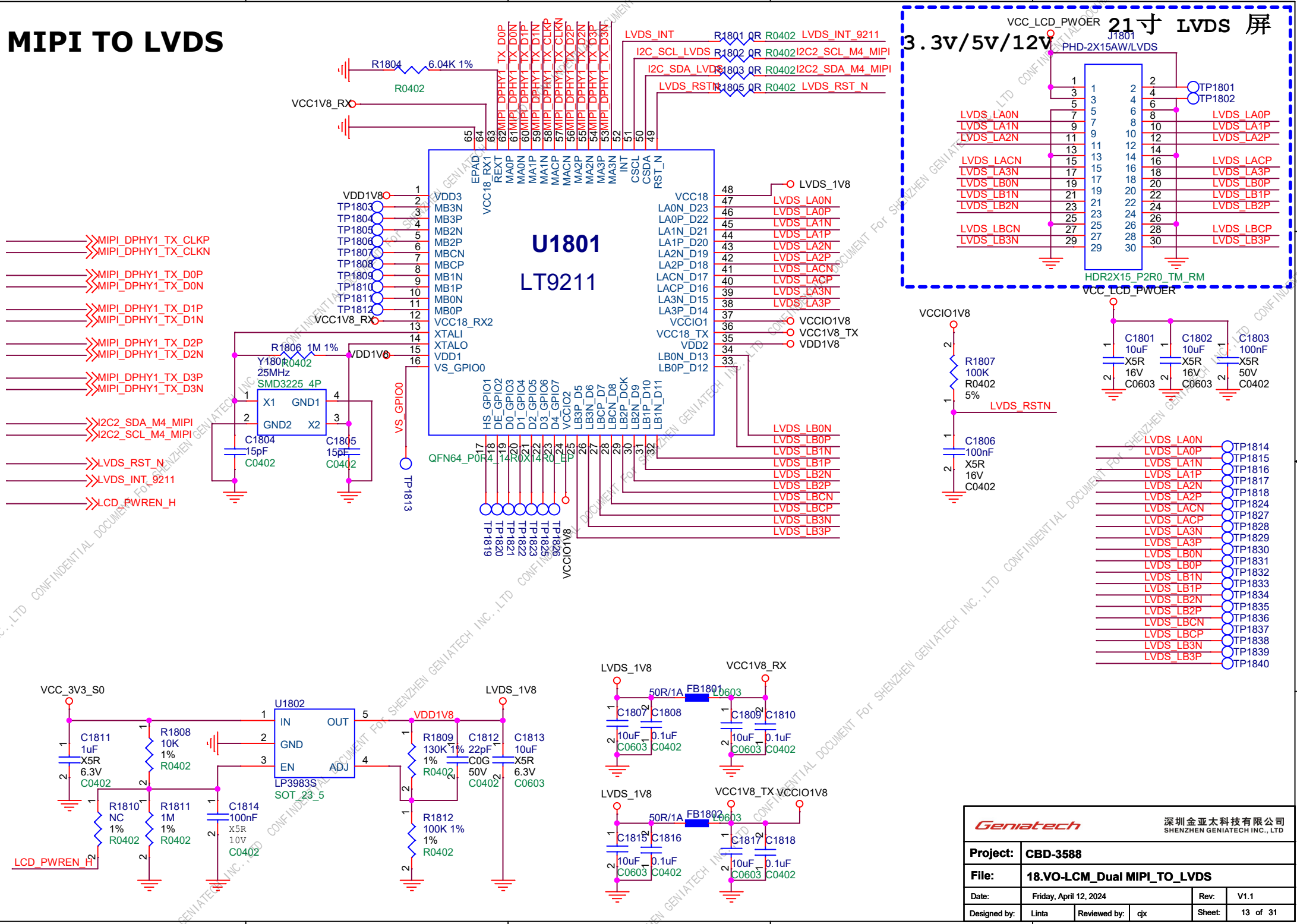
Single-MIPI0 LCM



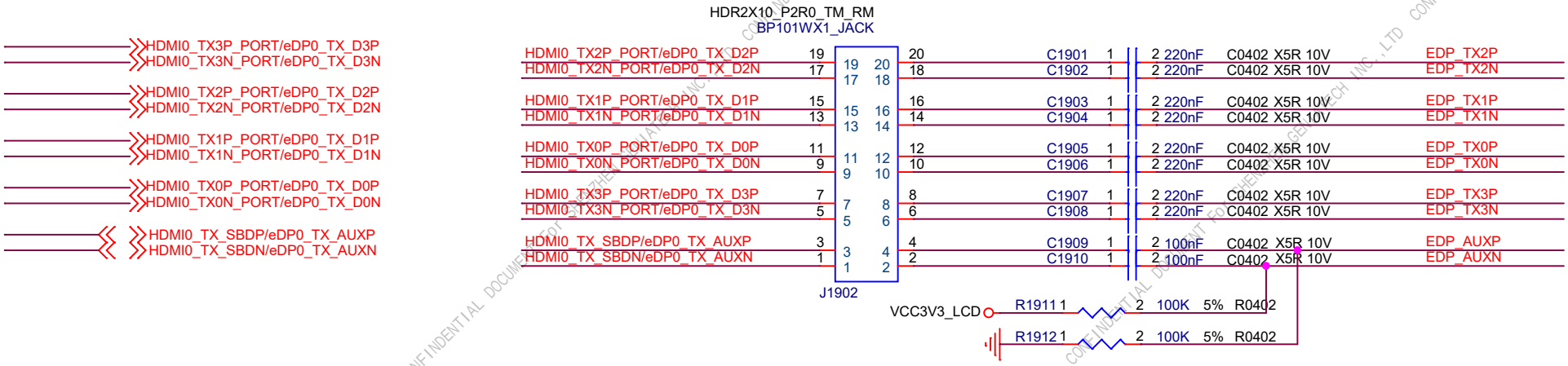
Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	CBD-3588				
File:	17.VO-LCM_Signel_MIPI_D/CPHY_TX				
Date:	Friday, April 12, 2024			Rev:	V1.1
Designed by:	Linta	Reviewed by:	cjx	Sheet:	12 of 31

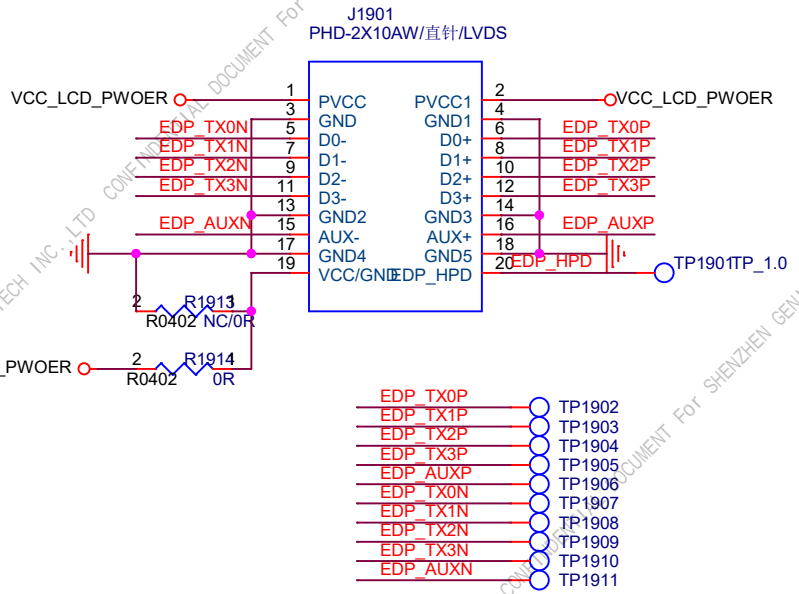
MIPI TO LVDS

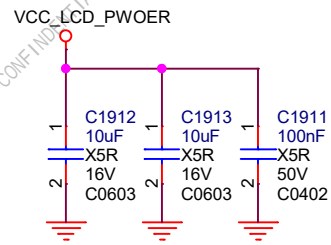


Geniatech	深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD				
Project:	CBD-3588				
File:	18.VO-LCM_Dual MIPI_TO_LVDS				
Date:	Friday, April 12, 2024			Rev:	V1.1
Designed by:	Linta	Reviewed by:	cjx	Sheet:	13 of 31

eDP LCD

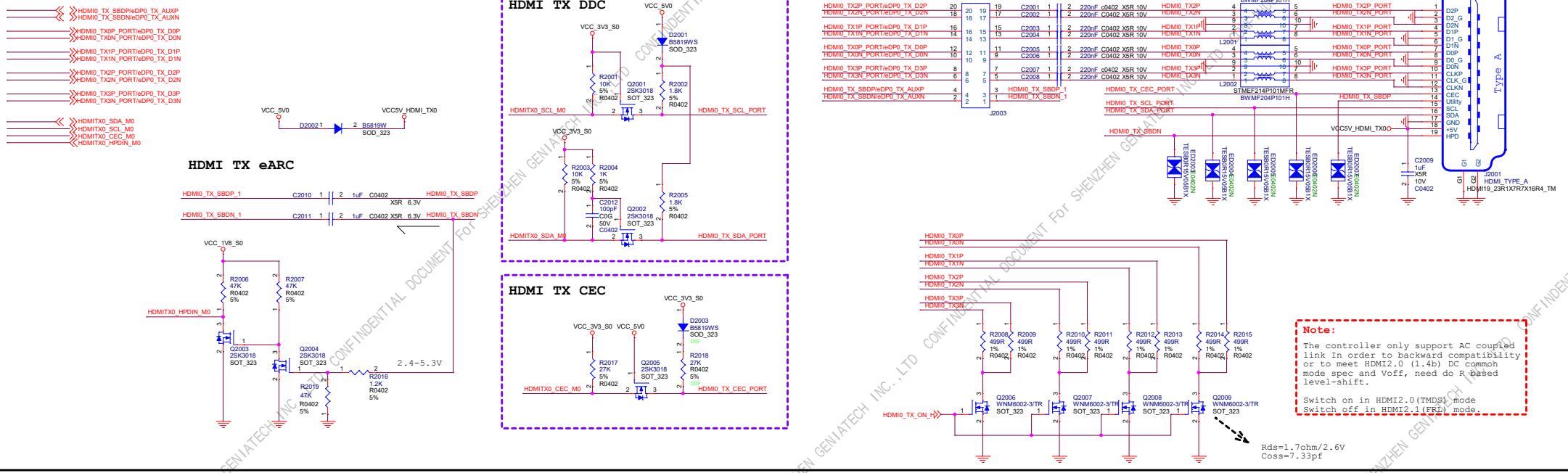




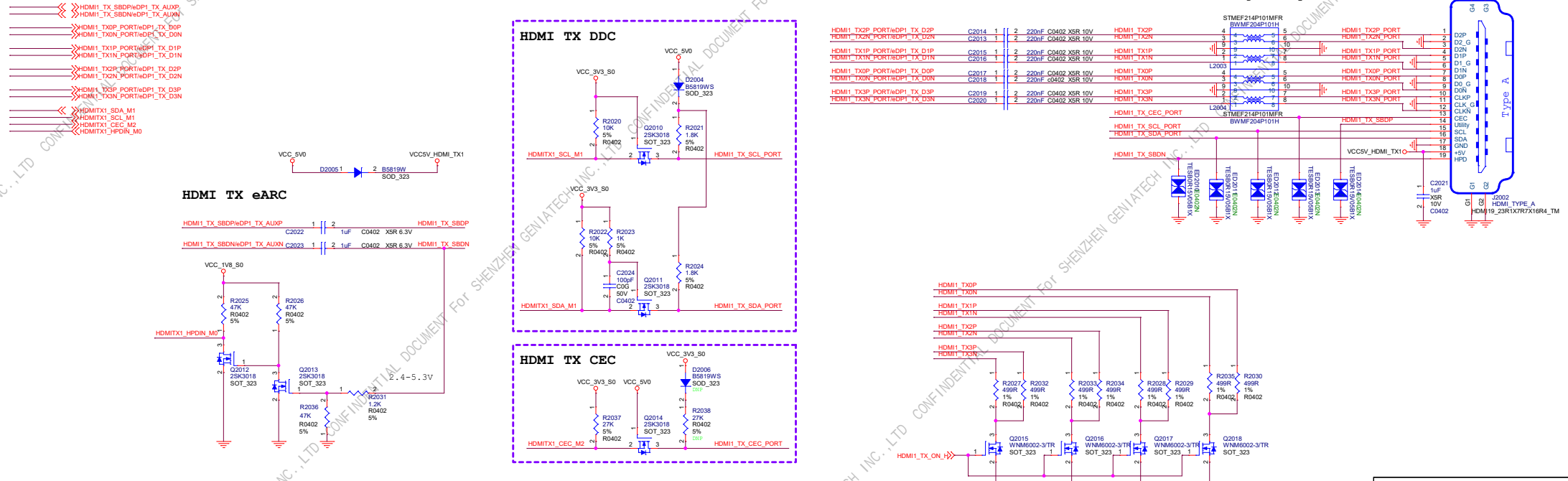


Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	CBD-3588				
File:	19.VO-LCM_eDP				
Date:	Friday, April 12, 2024			Rev:	V1.1
Designed by:	Linta	Reviewed by:	cjx	Sheet:	14 of 31

HDMI TX0

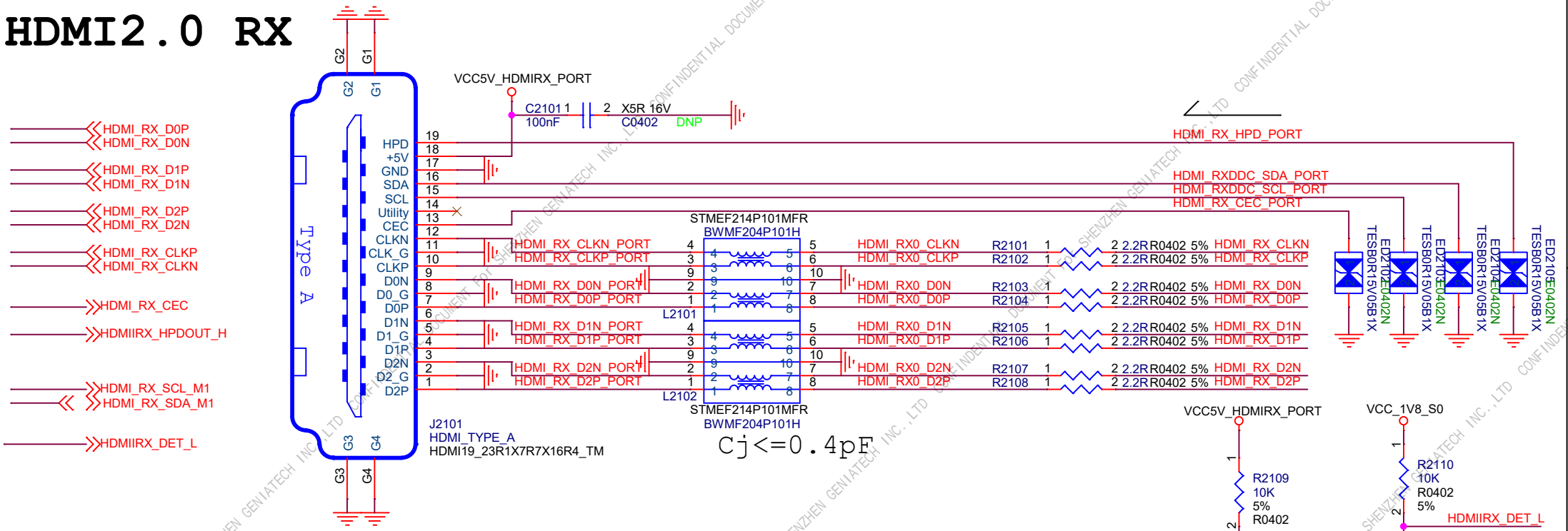


HDMI TX1

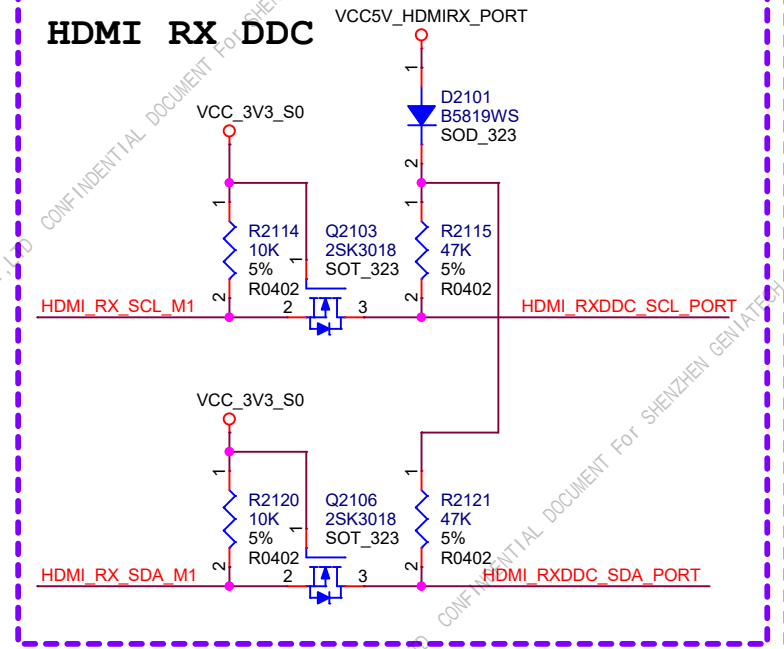


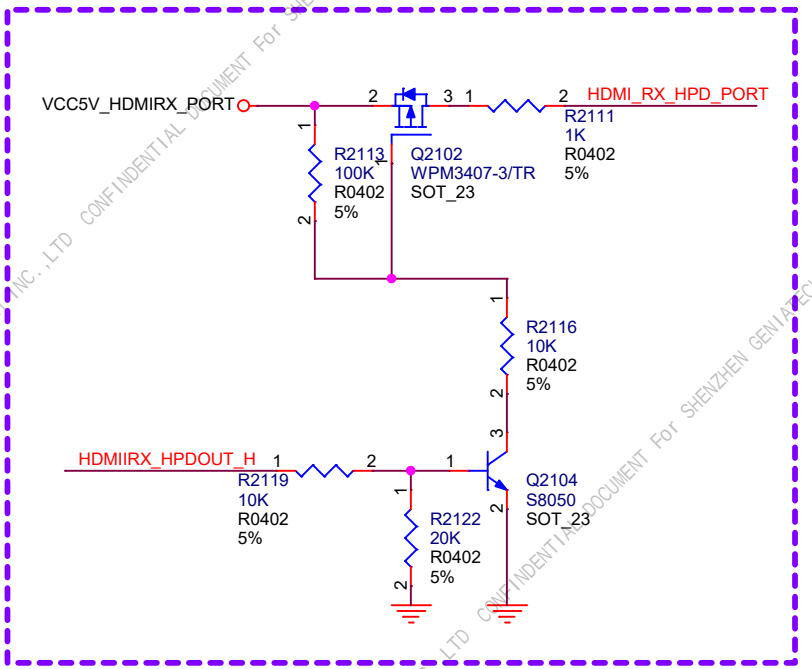
Geniatech	深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD		
Project:	CBD-3588		
File:	20.VO-HDMI2.1 TX		
Date:	Thursday, April 11, 2024	Rev:	V1.1
Designed by:	Linta	Reviewed by:	cjx
		Sheet:	15 of 31

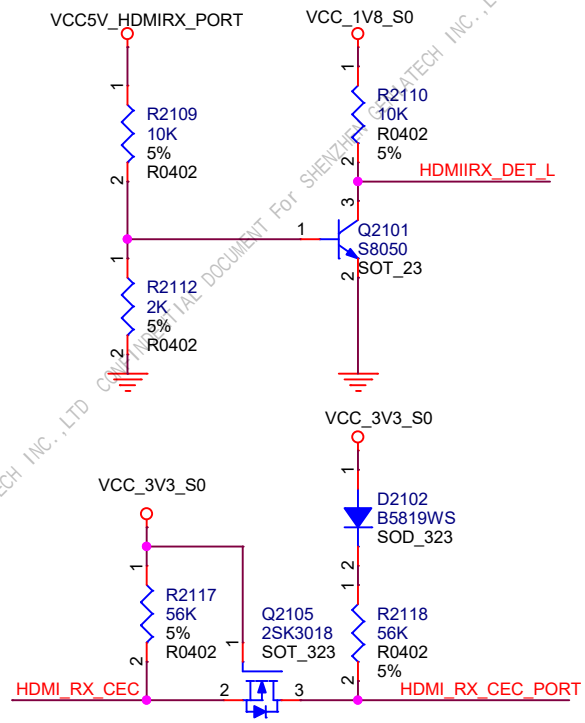
HDMI2.0 RX



HDMI RX DDC



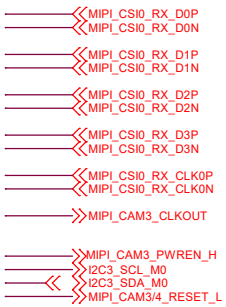


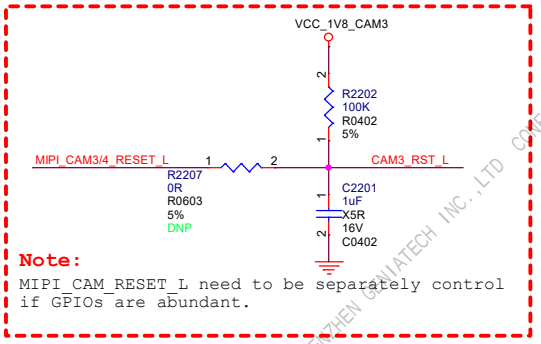


HPD:
Sink Side: Require output, Min 2.4V; Max 5.3V
Source Side:Require input and Detection.
Min 2.0V,Max:5.3V

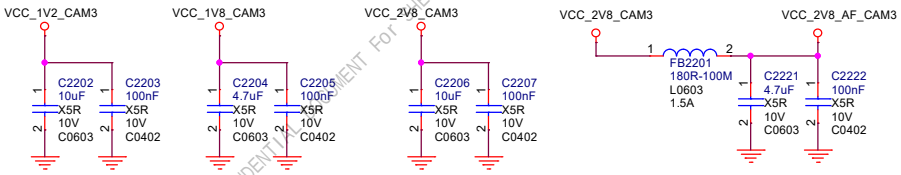
Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	CBD-3588				
File:	21.VI-HDMI2.0 RX				
Date:	Thursday, April 11, 2024			Rev:	V1.1
Designed by:	Linta	Reviewed by:	cjx	Sheet:	16 of 31

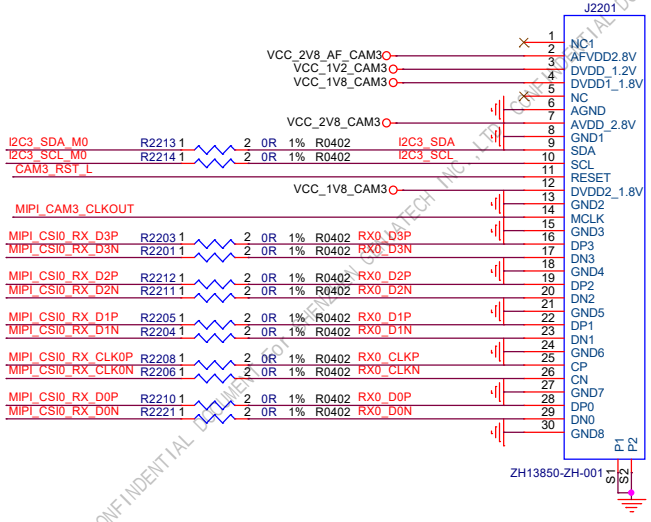
MIPI-DPHY0_RX

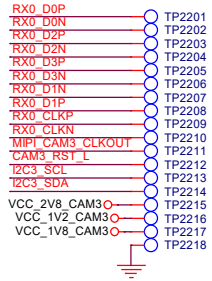


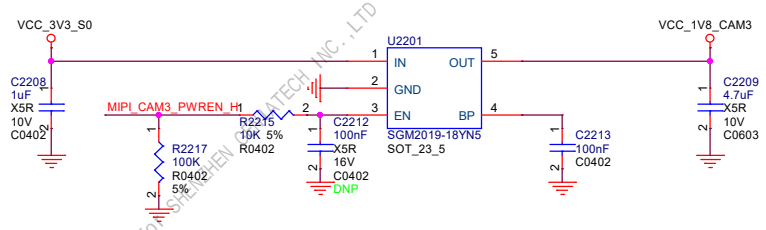


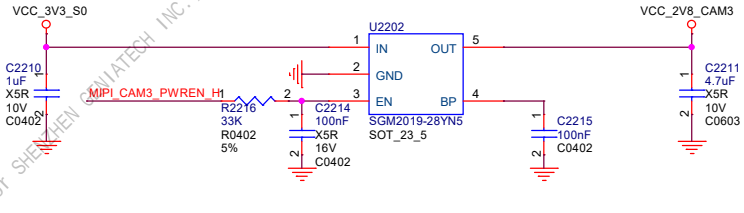
Note:
MIPI_CAM_RESET_L need to be separately control if GPIOs are abundant.

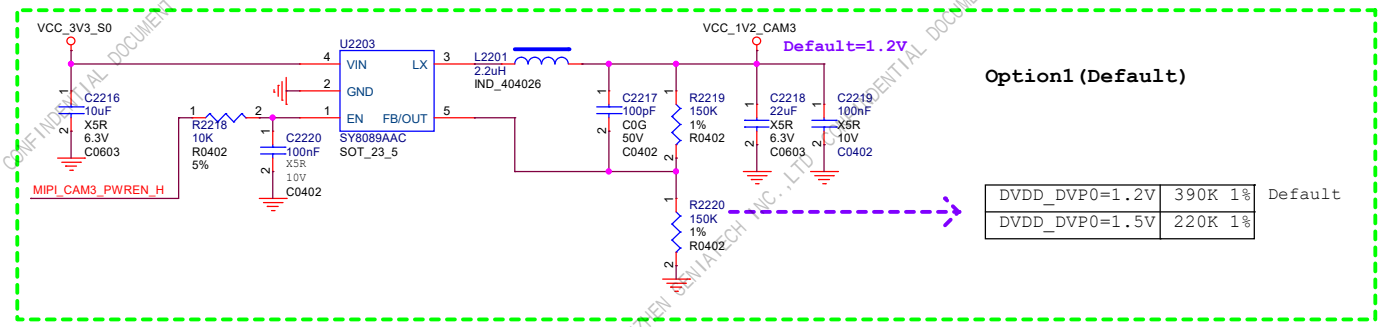










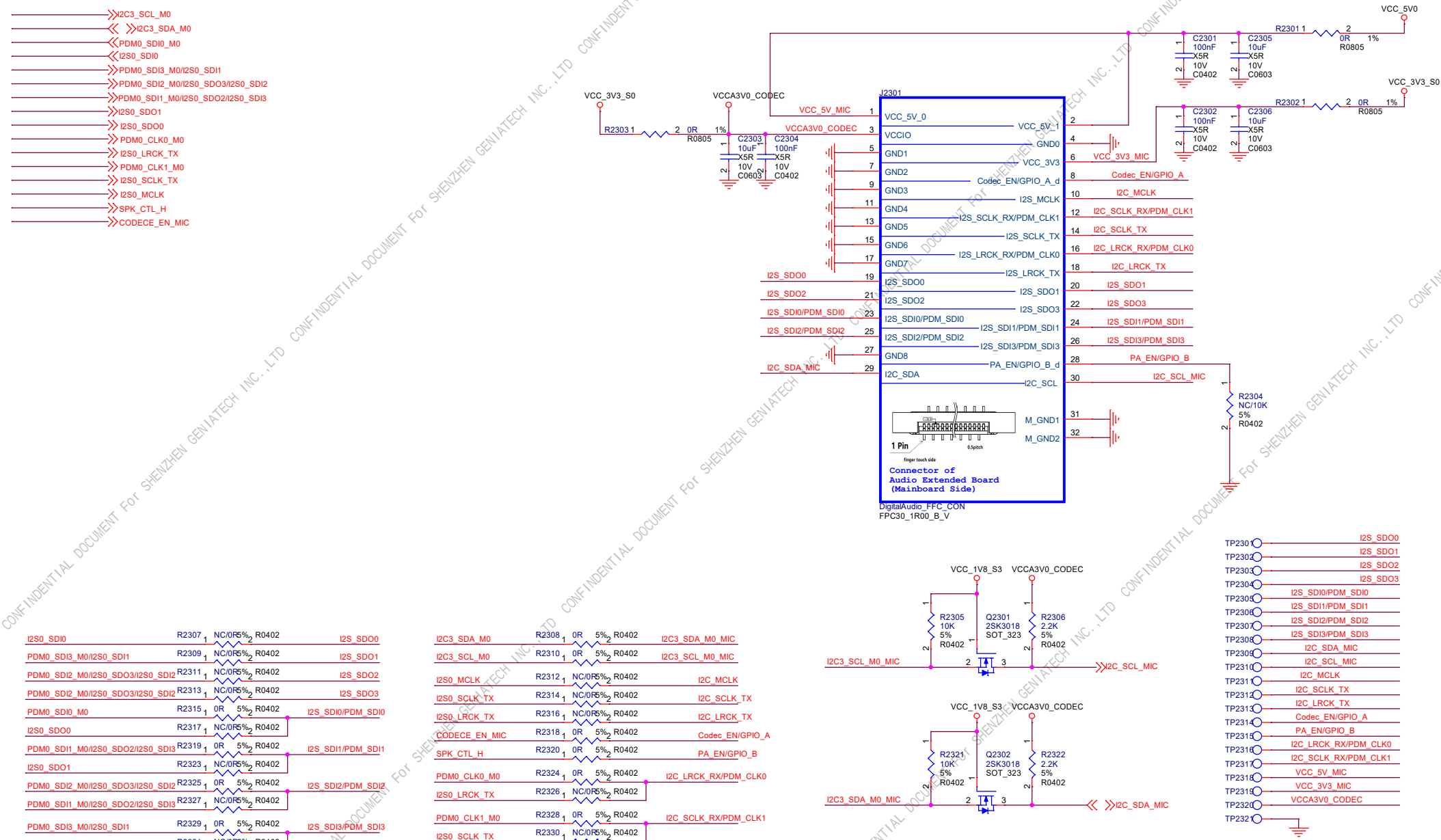


Option1(Default)

DVDD_DVP0=1.2V	390K 1%	Default
DVDD_DVP0=1.5V	220K 1%	

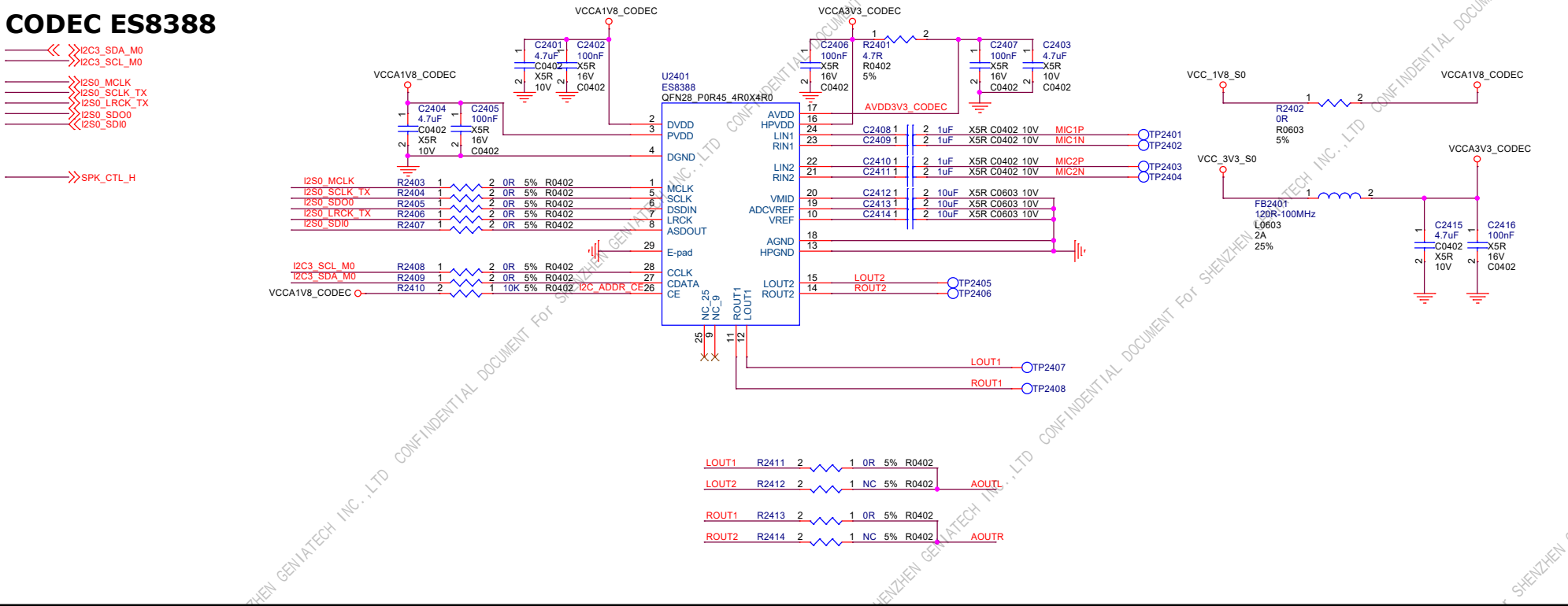
Note:
Adjust the power on sequence according to the camera model
eg:GC8034
Power on Sequence
1.8V-->1.2V-->2.8V--->MCLK-->PWDN--->RST

Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	CBD-3588				
File:	22.VI-Camera_MIPI_DPHY0-RX				
Date:	Friday, April 12, 2024			Rev:	V1.1
Designed by:	Linta	Reviewed by:	cjx	Sheet:	17 of 31

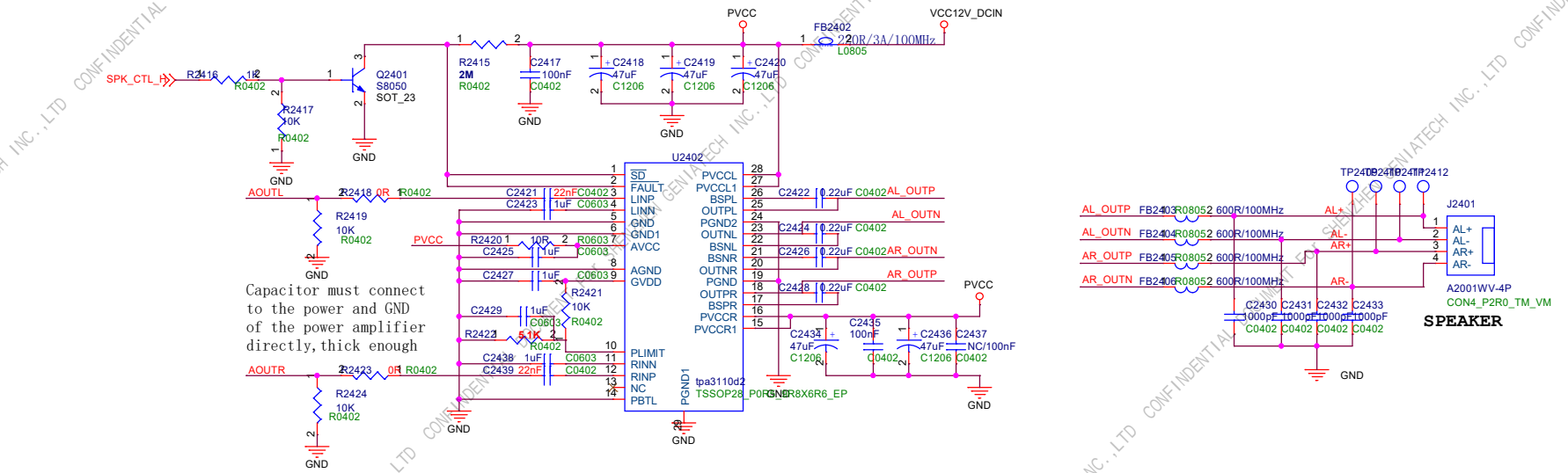


Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	CBD-3588				
File:	23.Audio-MIC ArrayInterface				
Date:	Friday, April 12, 2024			Rev:	V1.1
Designed by:	Linta	Reviewed by:	cjx	Sheet:	18 of 31

CODEC ES8388

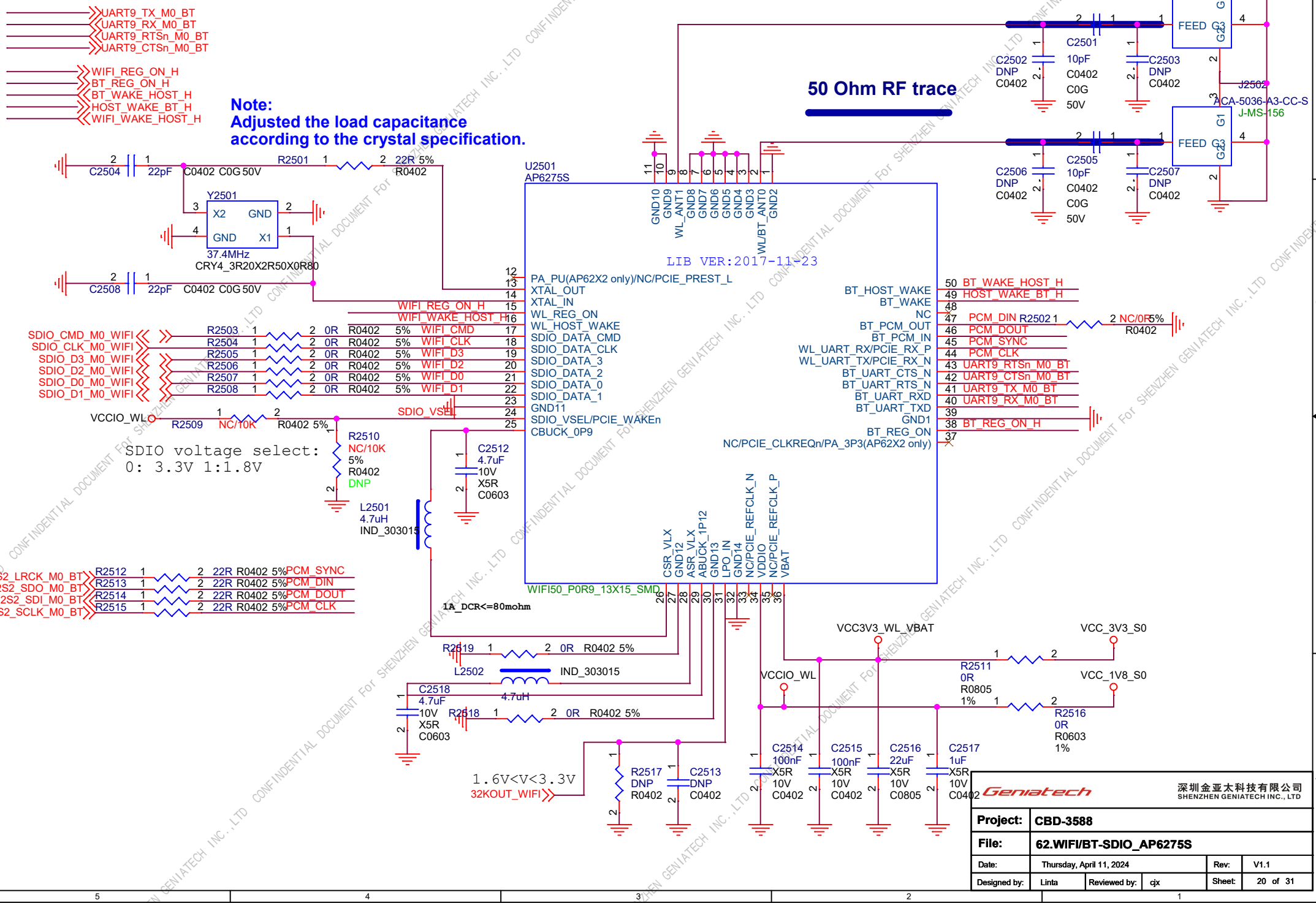


SPEAKER



Geniatech	深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD				
Project:	CBD-3588				
File:	26.PCIE-M.2_B&M KEY				
Date:	Friday, April 12, 2024			Rev:	V1.1
Designed by:	Linta	Reviewed by:	cjx	Sheet:	19 of 31

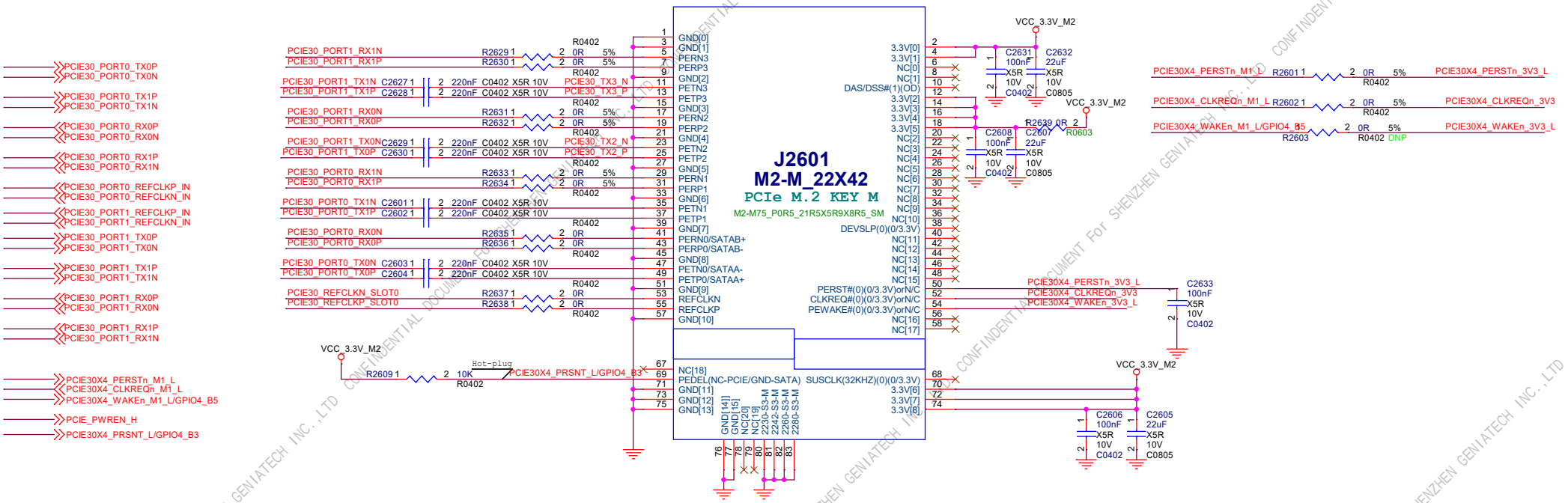
WIFI（802.11 a/b/g/n/ac 2x2 MIMO）



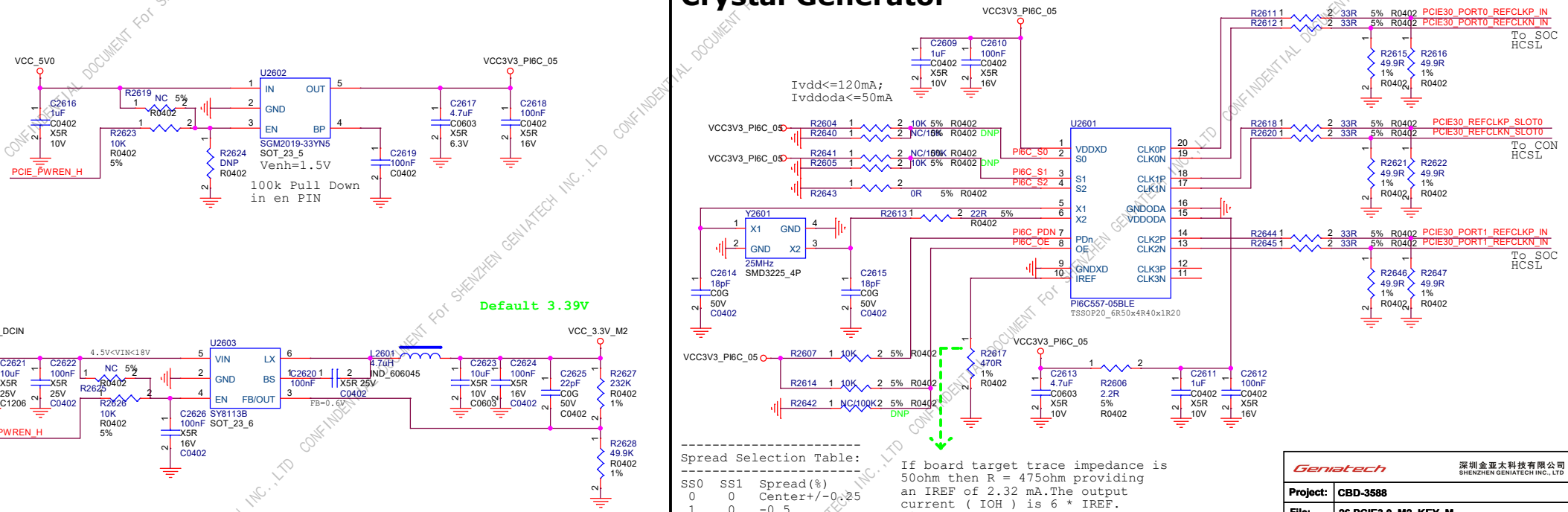
Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	CBD-3588				
File:	62.WIFI/BT-SDIO_AP6275S				
Date:	Thursday, April 11, 2024			Rev:	V1.1
Designed by:	Linta	Reviewed by:	cjx	Sheet:	20 of 31

PCIe3.0 x 4 Slot

PCIe2 M2_KEY_M



Crystal Generator



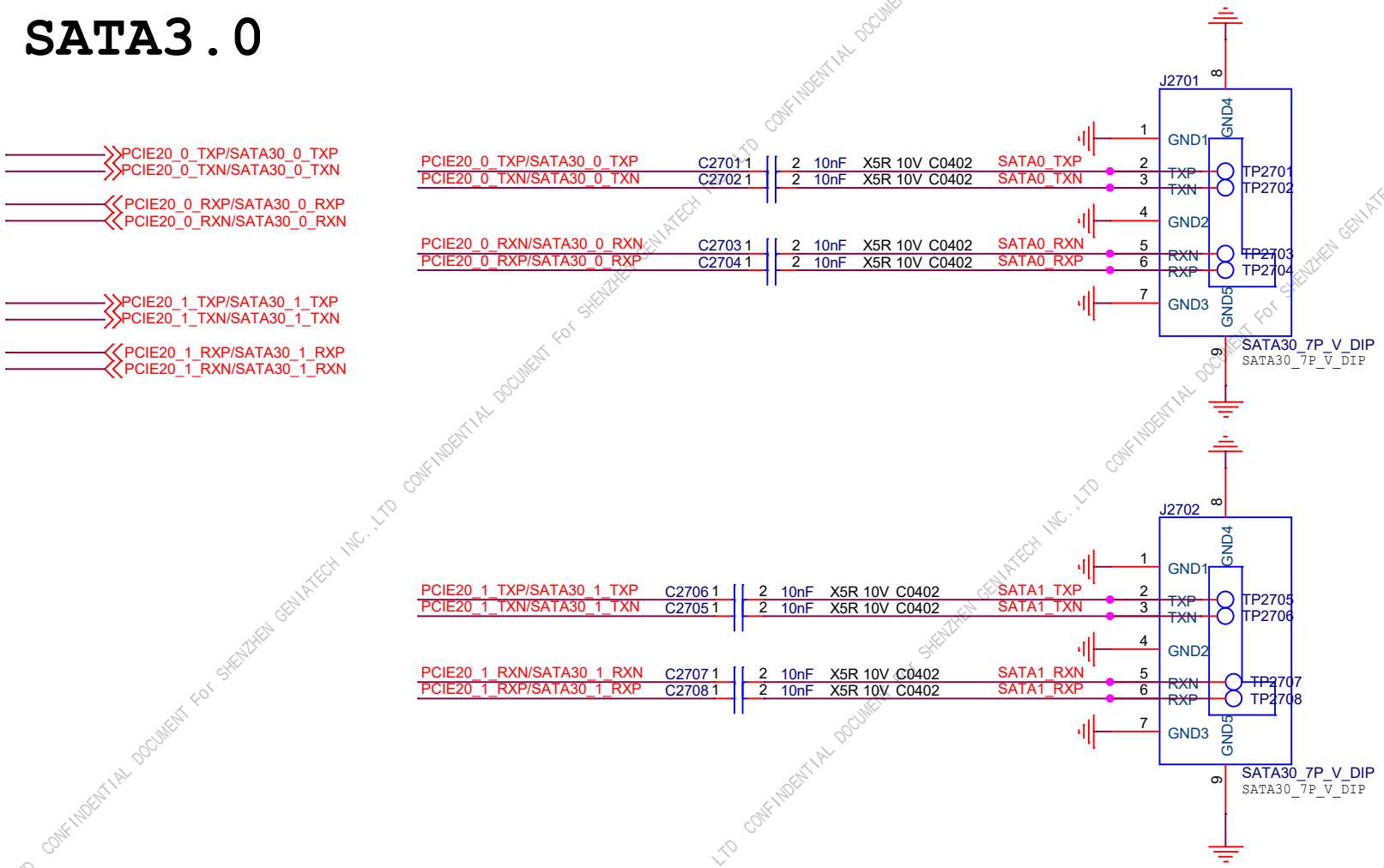
Spread Selection Table:

SS0	SS1	Spread(%)
0	0	Center+/-0.25
1	0	-0.5
0	1	-0.75
1	1	No Spread

If board target trace impedance is 50ohm then R = 475ohm providing an IREF of 2.32 mA.The output current (IOH) is 6 * IREF.
Vih=6x2.32X50=696mV

Geniatech	深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD		
Project:	CBD-3588		
File:	26.PCIE3.0_M2_KEY_M		
Date:	Thursday, April 11, 2024	Rev:	V1.1
Designed by:	Linta	Reviewed by: cjx	Sheet: 21 of 31

SATA3.0



Geniatech	深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD				
Project:	CBD-3588				
File:	27SATA-SATA3.0 Slot_7P				
Date:	Friday, April 12, 2024			Rev:	V1.1
Designed by:	Linta	Reviewed by:	cjx	Sheet:	22 of 31

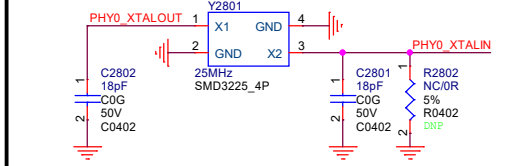
RGMII TO RJ45

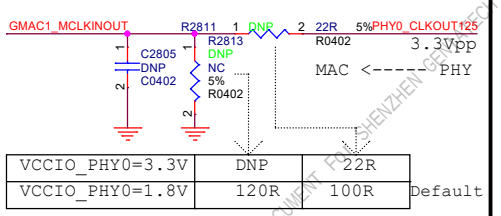
GMAC1_TXD0
GMAC1_TXD1
GMAC1_TXD2
GMAC1_TXD3
GMAC1_TXEN
GMAC1_TXCLK

GMAC1_RXD0
GMAC1_RXD1
GMAC1_RXD2
GMAC1_RXD3
GMAC1_RXDV_CRS

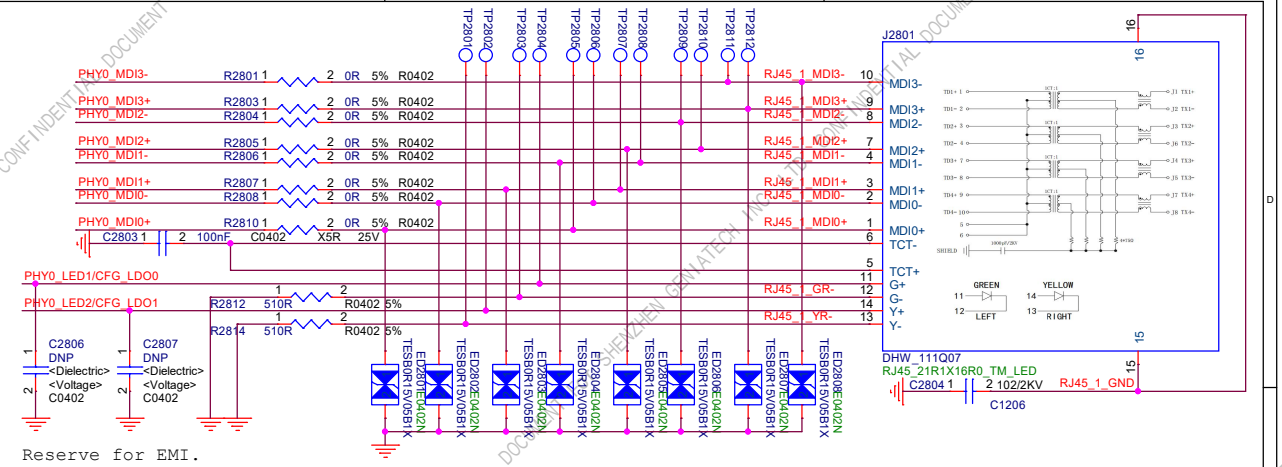
GMAC1_RXCLK
ETH1_REFCLKO_25M
GMAC1_MCLKINOUT
GMAC1_MDC
GMAC1_MDIO

GMAC1_RSTn_L

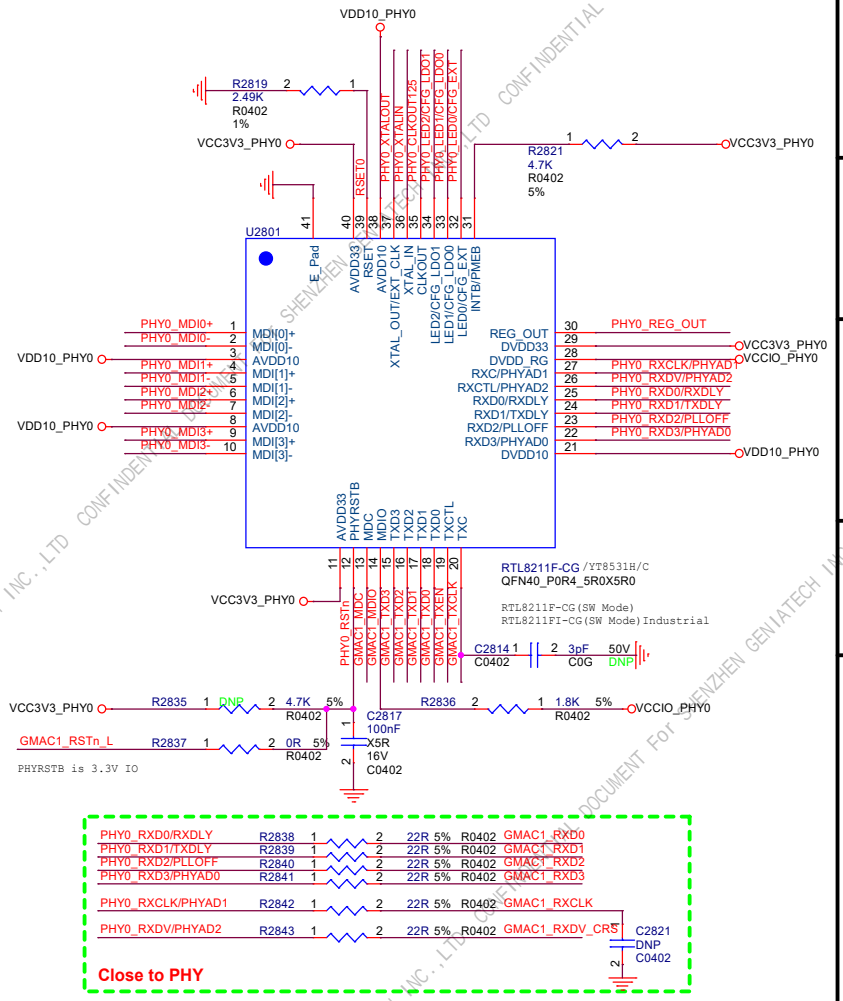


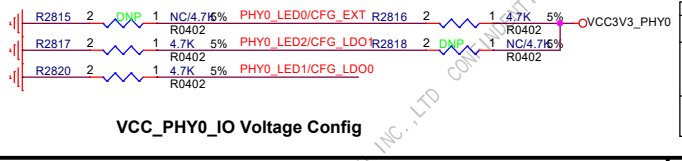


VCCIO_PHY0=3.3V	DNP	22R
VCCIO_PHY0=1.8V	120R	100R Default



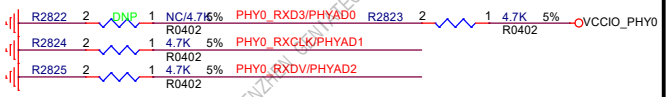
Reserve for EMI.





VCC_PHY0_IO Voltage Config

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V(default)	1'b1	2'b00	CFG_EXT: 1:External Power Source for IO pad. 0:Integrated LDO for IO pad CFG_LDO(1:0) 10:1.8V 00:3.3V
External 1.8V	1'b1	2'b10	
Internal 1.8V	1'b0	2'b10	

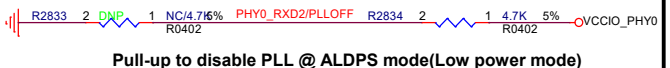


PHY Address Config

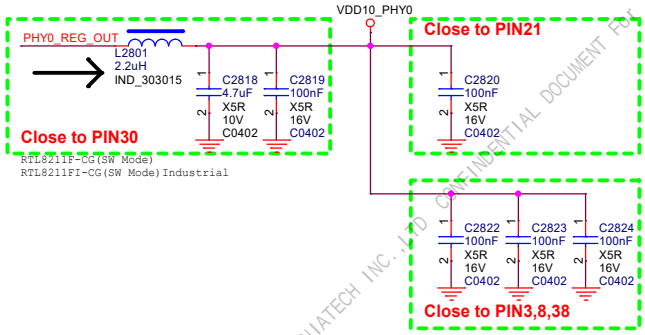
PHY Address	PHYAD[2:0]
1 (default)	3'b001

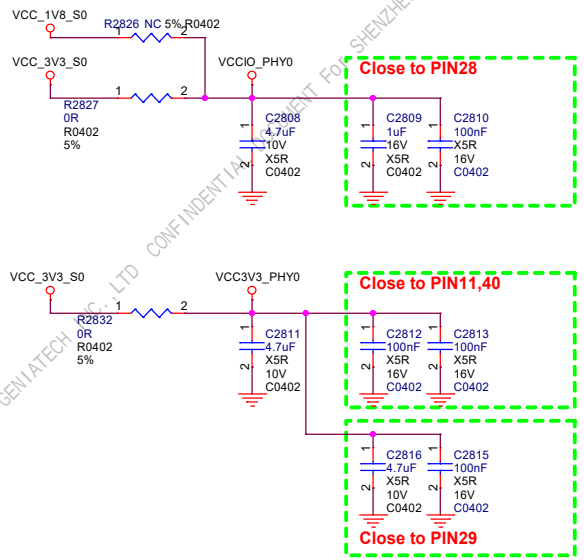
Pull-up for additional 2ns delay to RXC for data latching

Pull-up for additional 2ns delay to TXC for data latching



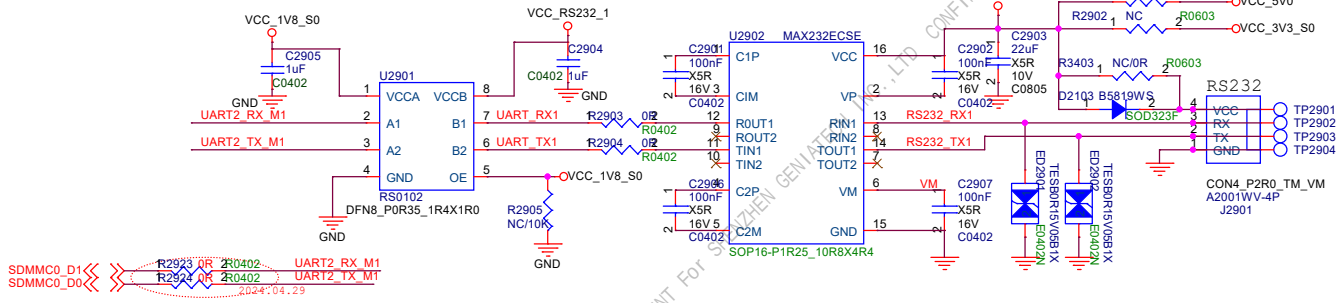
Pull-up to disable PLL @ ALDPS mode(Low power mode)



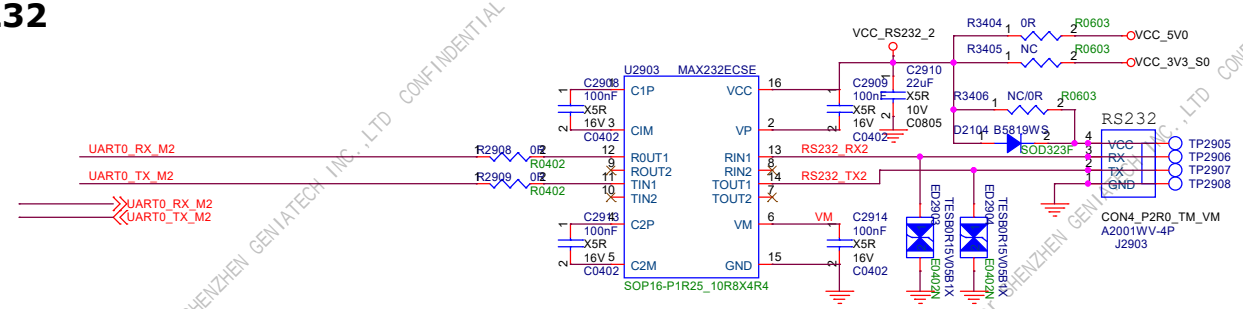


Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	CBD-3588				
File:	28.Ethernet-GPHY_RGMII1				
Date:	Friday, April 12, 2024			Rev:	V1.1
Designed by:	Linta	Reviewed by:	cjx	Sheet:	23 of 31

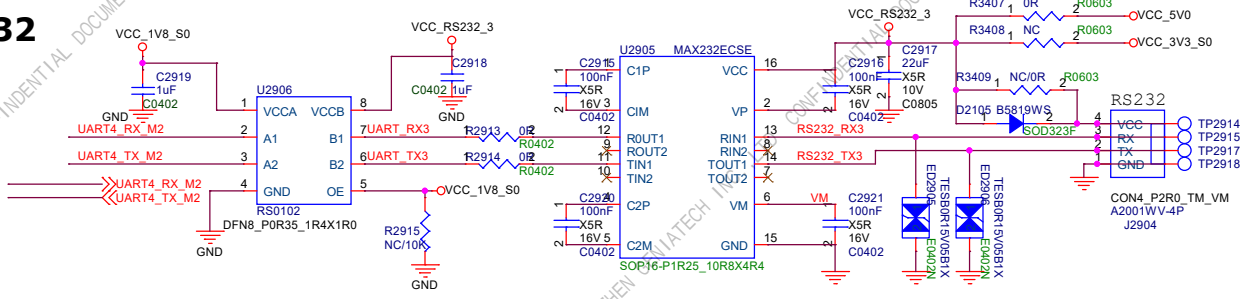
RS232



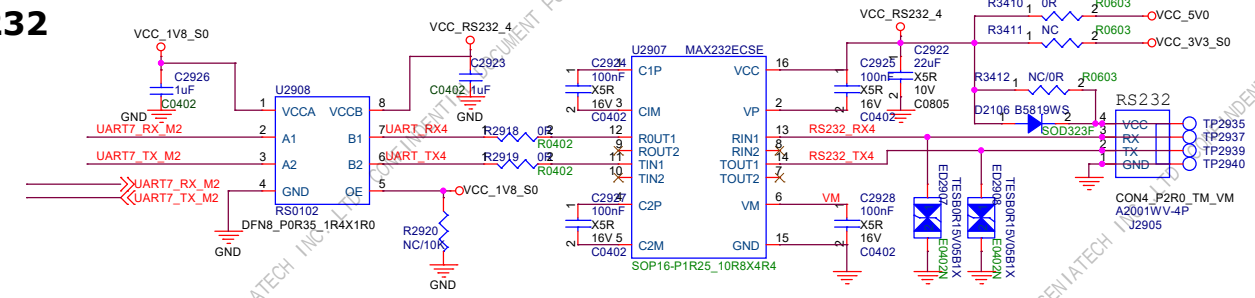
RS232



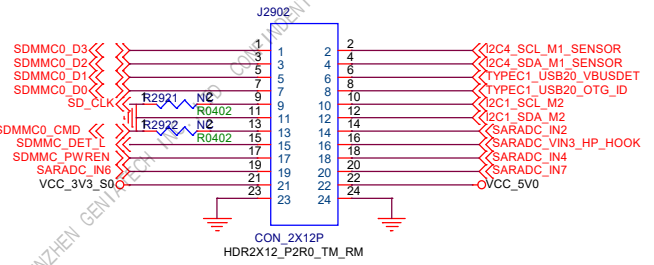
RS232

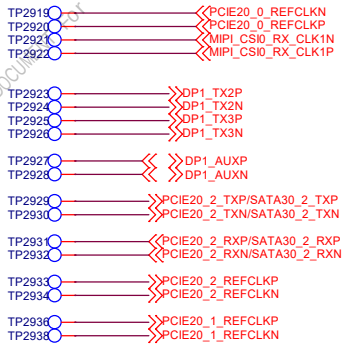


RS232



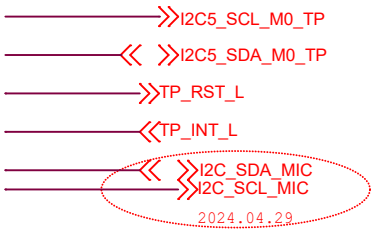
GPIOs

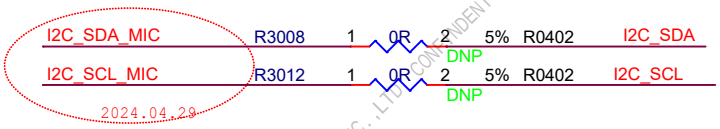


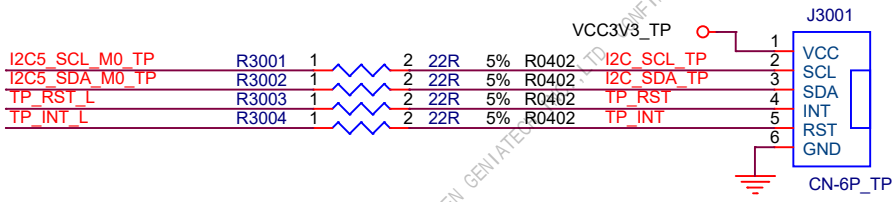


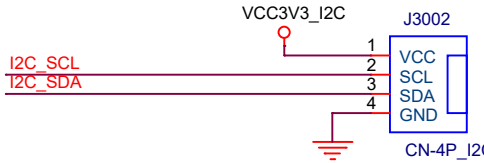
Geniatech	深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD				
Project:	CBD-3588				
File:	29.RS232&GPIO				
Date:	Friday, April 12, 2024			Rev:	V1.1
Designed by:	Linta	Reviewed by:	cjx	Sheet:	24 of 31

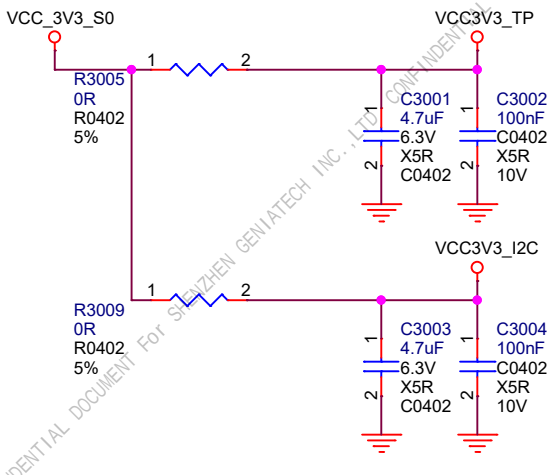
Touch Panel connector

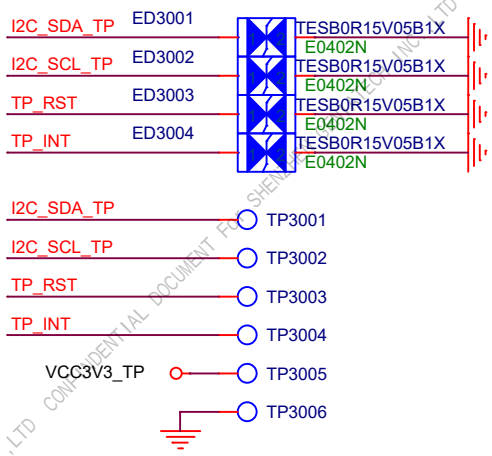


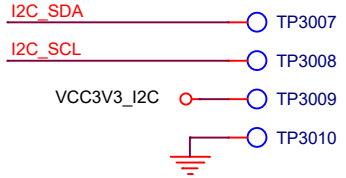






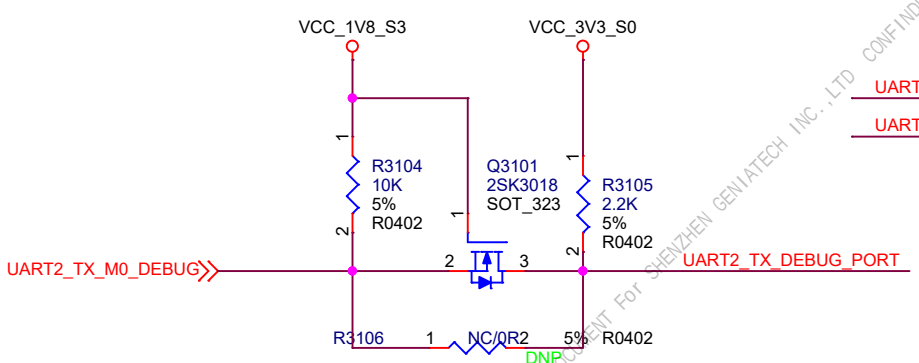


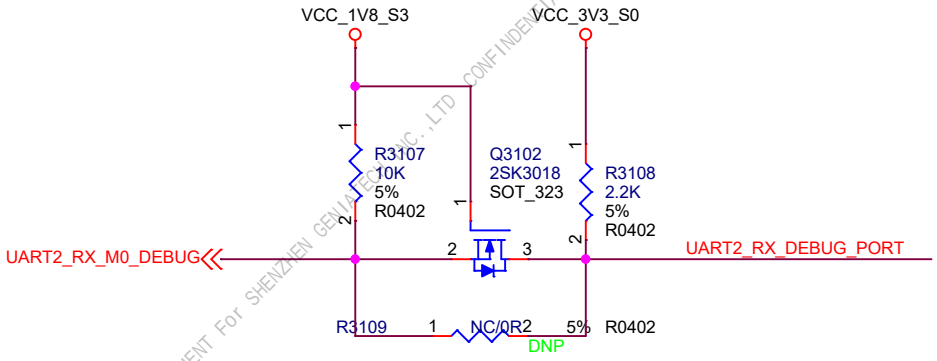


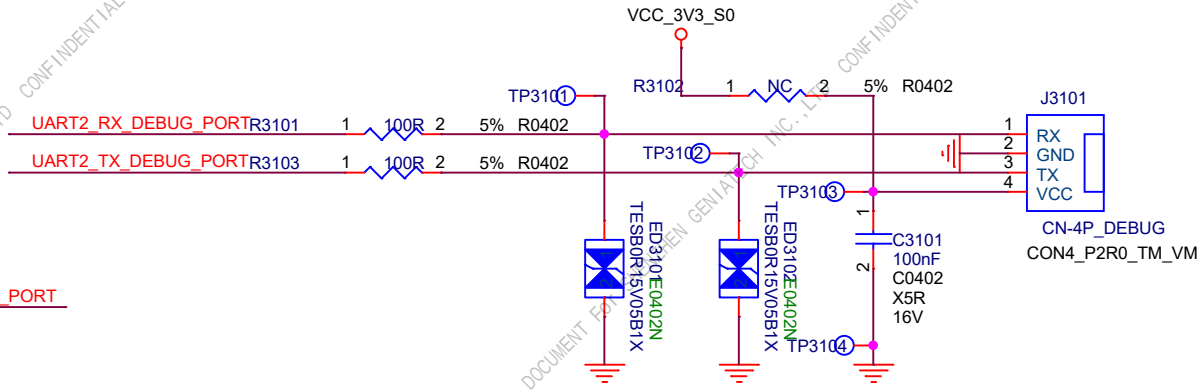


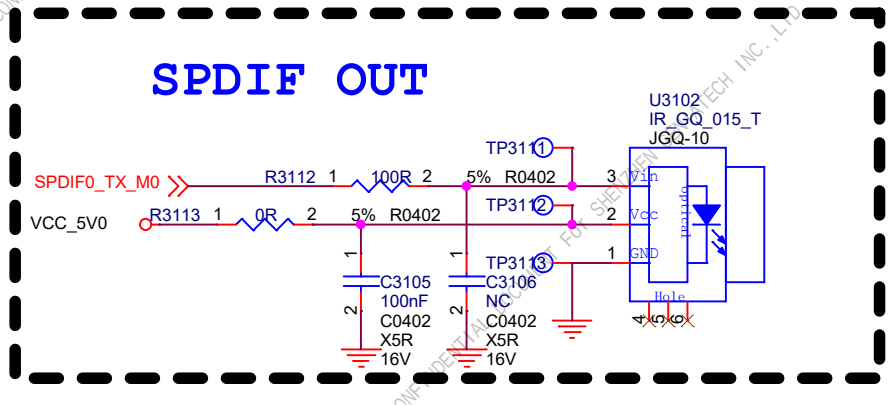
Geniatech	深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD				
Project:	CBD-3588				
File:	30.TP Connector_COF				
Date:	Friday, April 12, 2024			Rev:	V1.1
Designed by:	Linta	Reviewed by:	cjx	Sheet:	25 of 31

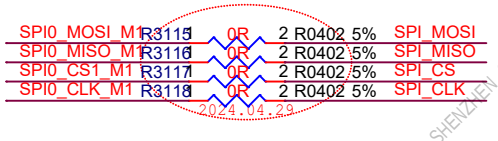
UART TO USB (DEBUG)

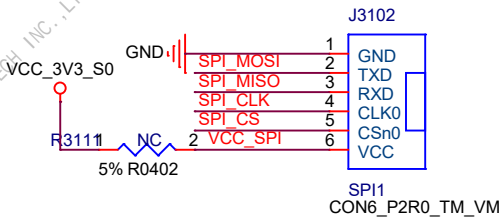












Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	CBD-3588				
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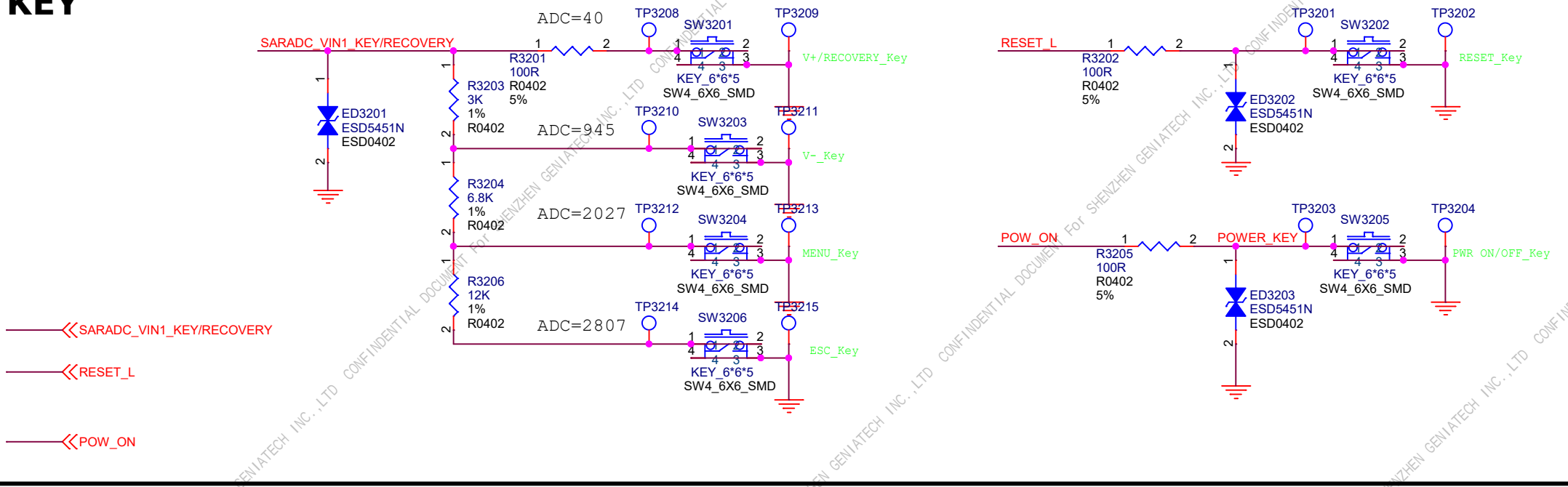
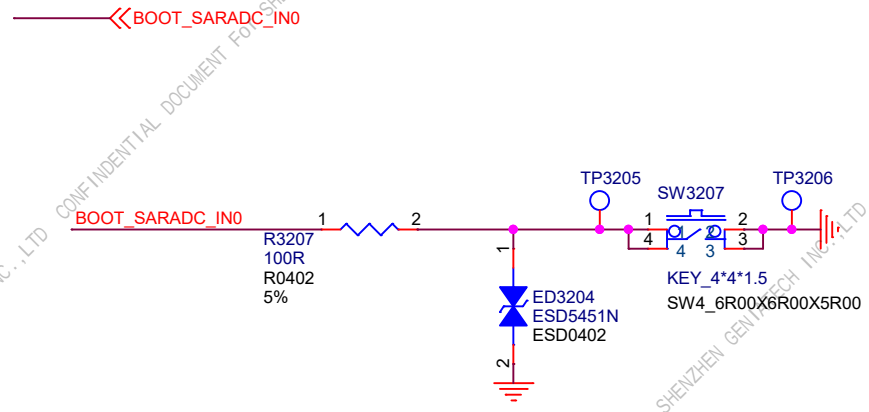
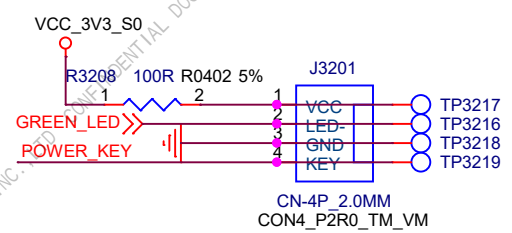
KEY







Note:

If BOOT_SARADC_IN0=0V after power-on reset, then system will enter into Maskrom mode.

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Project:	CBD-3588				
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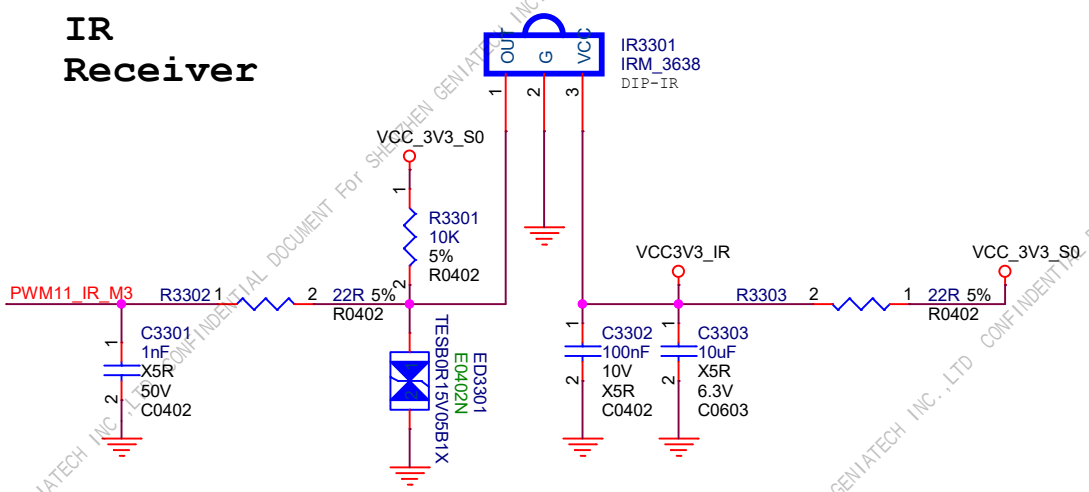
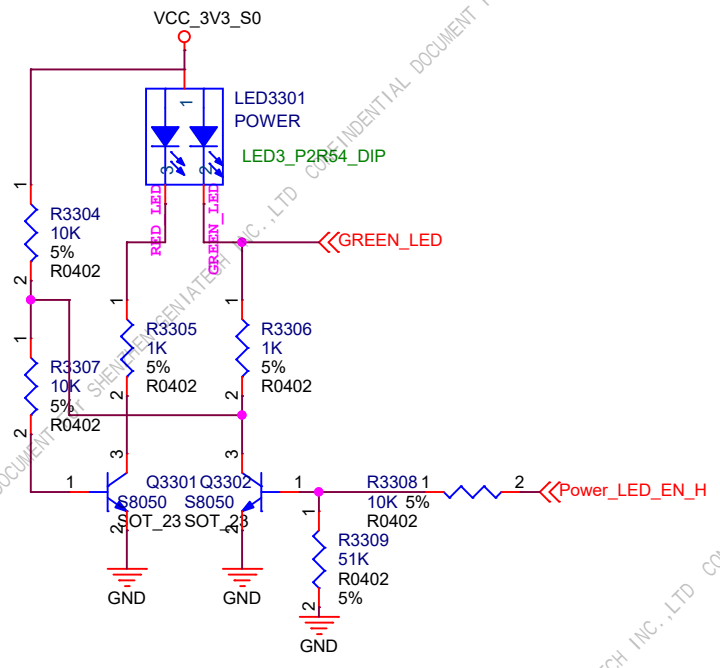
PWM11_IR_M3

IR Receiver





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Project:	CBD-3588				
File:	33.IR&LED				
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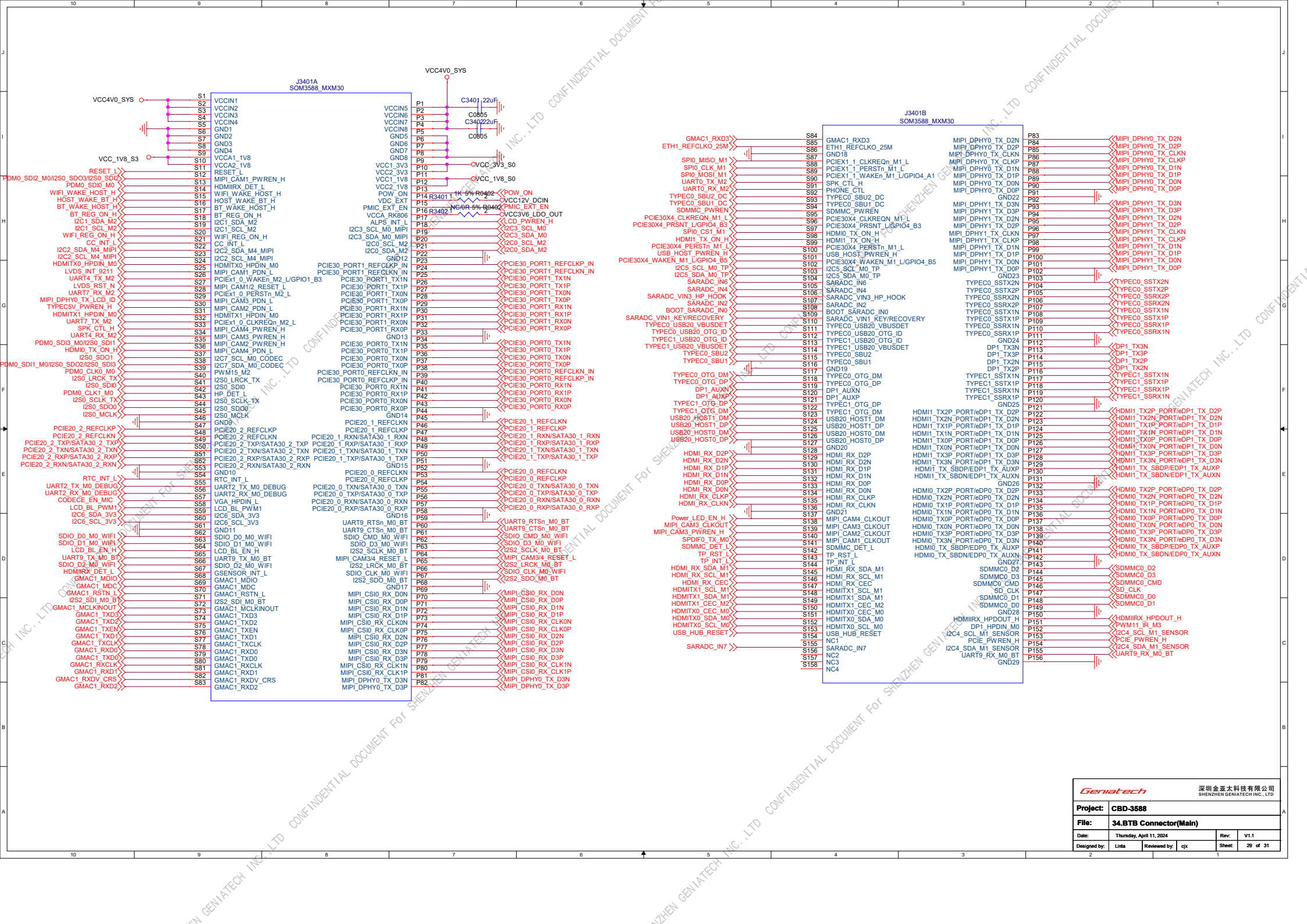
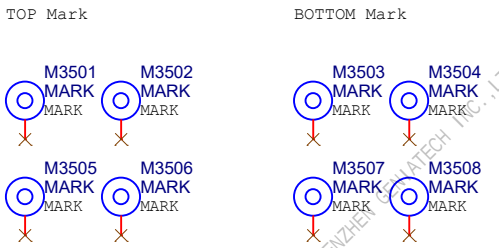
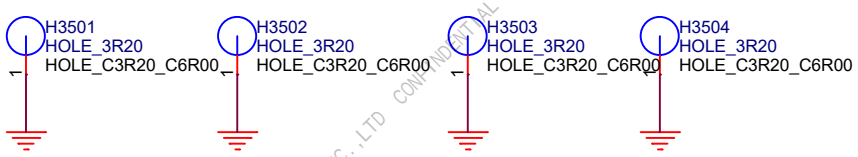


Mark



HOLE



Geniatech	深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD				
Project:	CBD-3588				
File:	35.Mark/Hole/Heatsink				
Date:	Thursday, April 11, 2024			Rev:	V1.1
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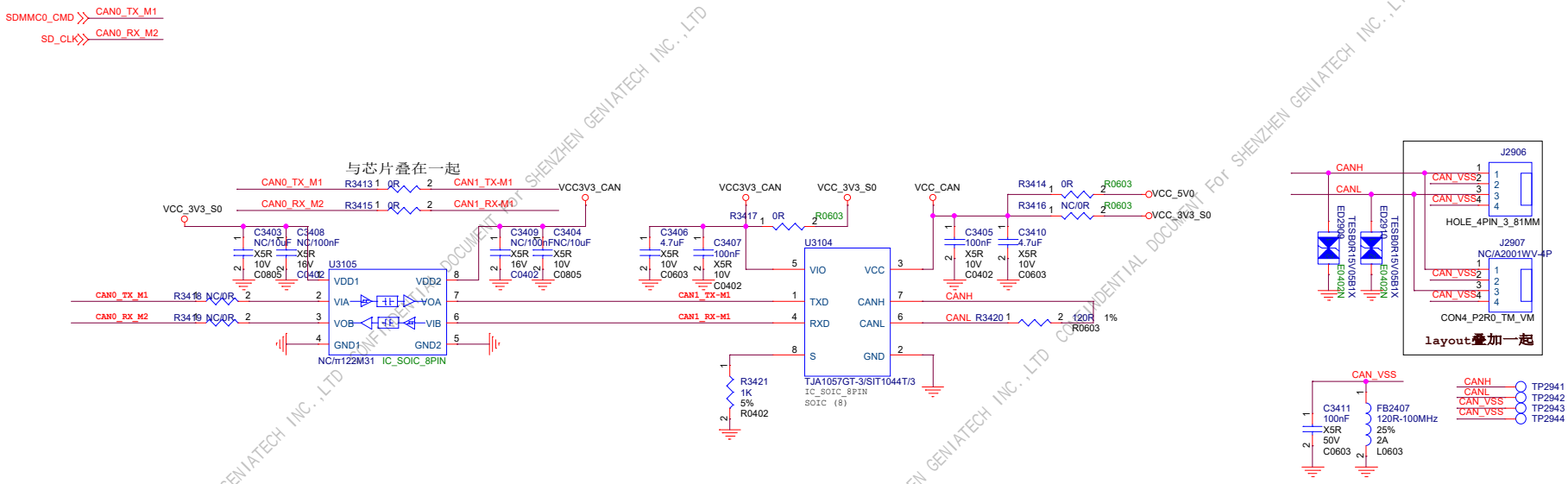

Geniatech	深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD				
Project:	**CBD-3588**				
File:	**36.CAN**				
Date:	Friday, April 12, 2024			Rev:	V1.1
Designed by:	Linta	Reviewed by:	cjx	Sheet:	31 of 31