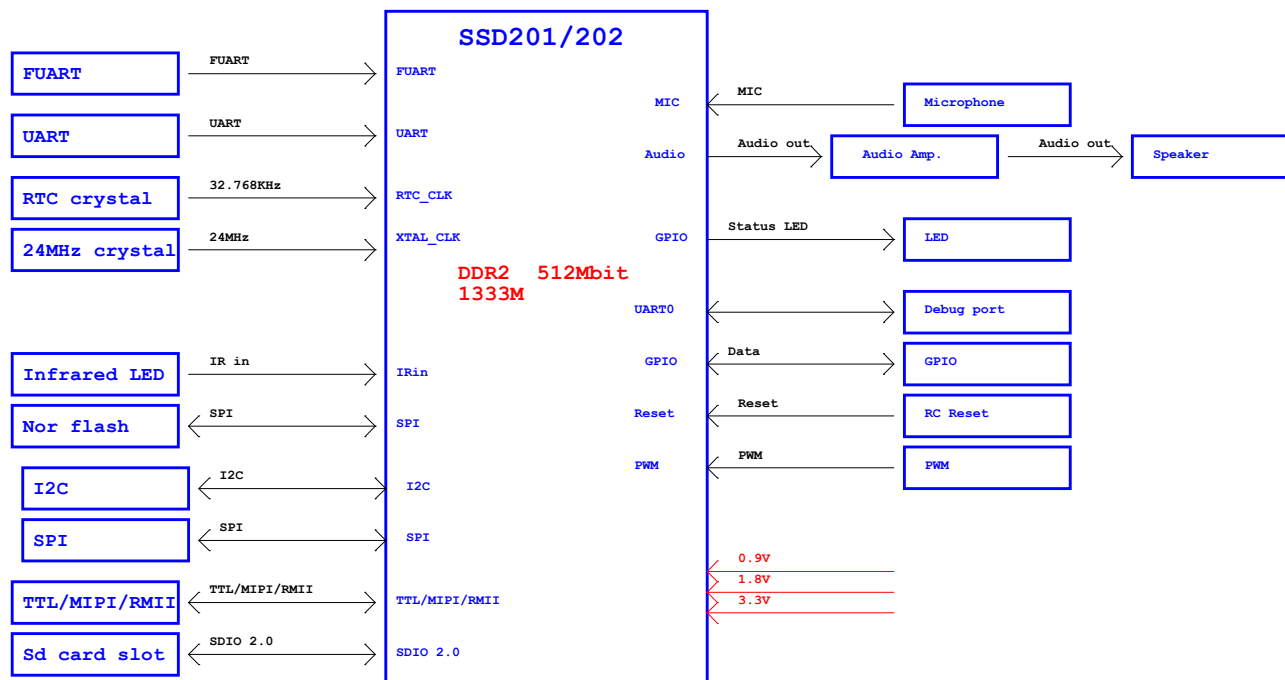
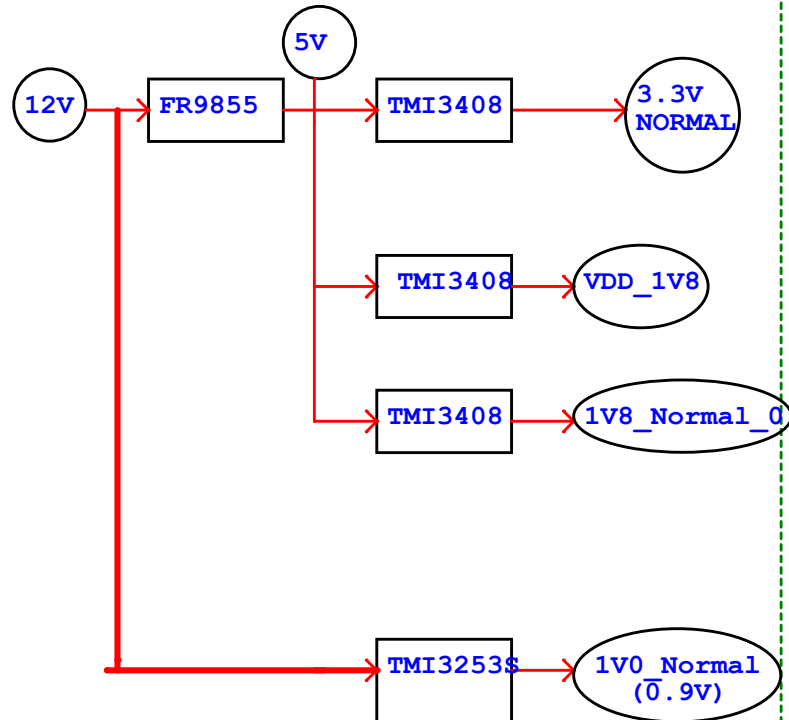




Power tree



Default 2x RJ45+MIPI/LVDS

Default RMII

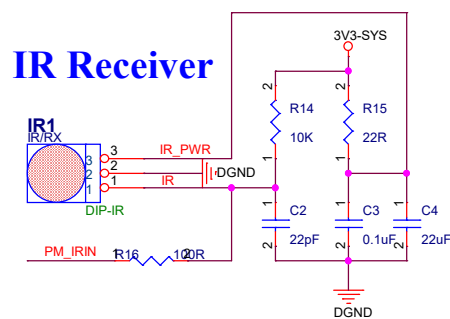
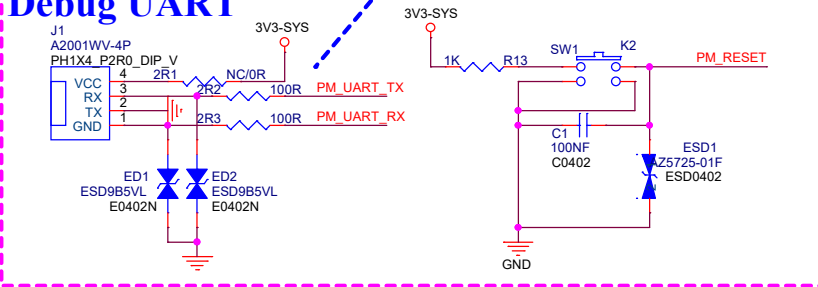
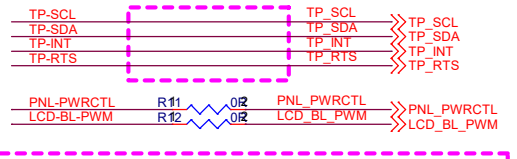
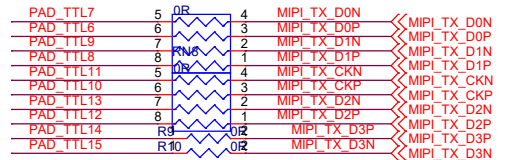
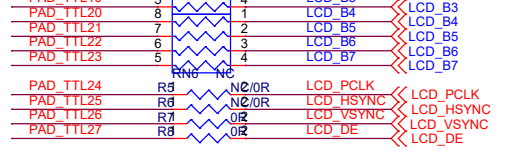
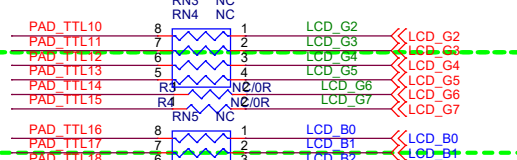
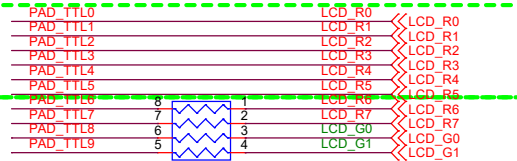
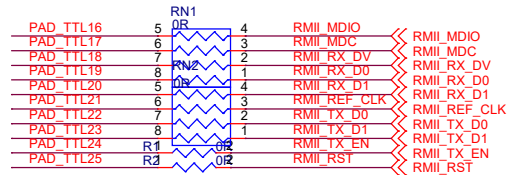
TF

RMII LAN

Default MIPI

Debug UART

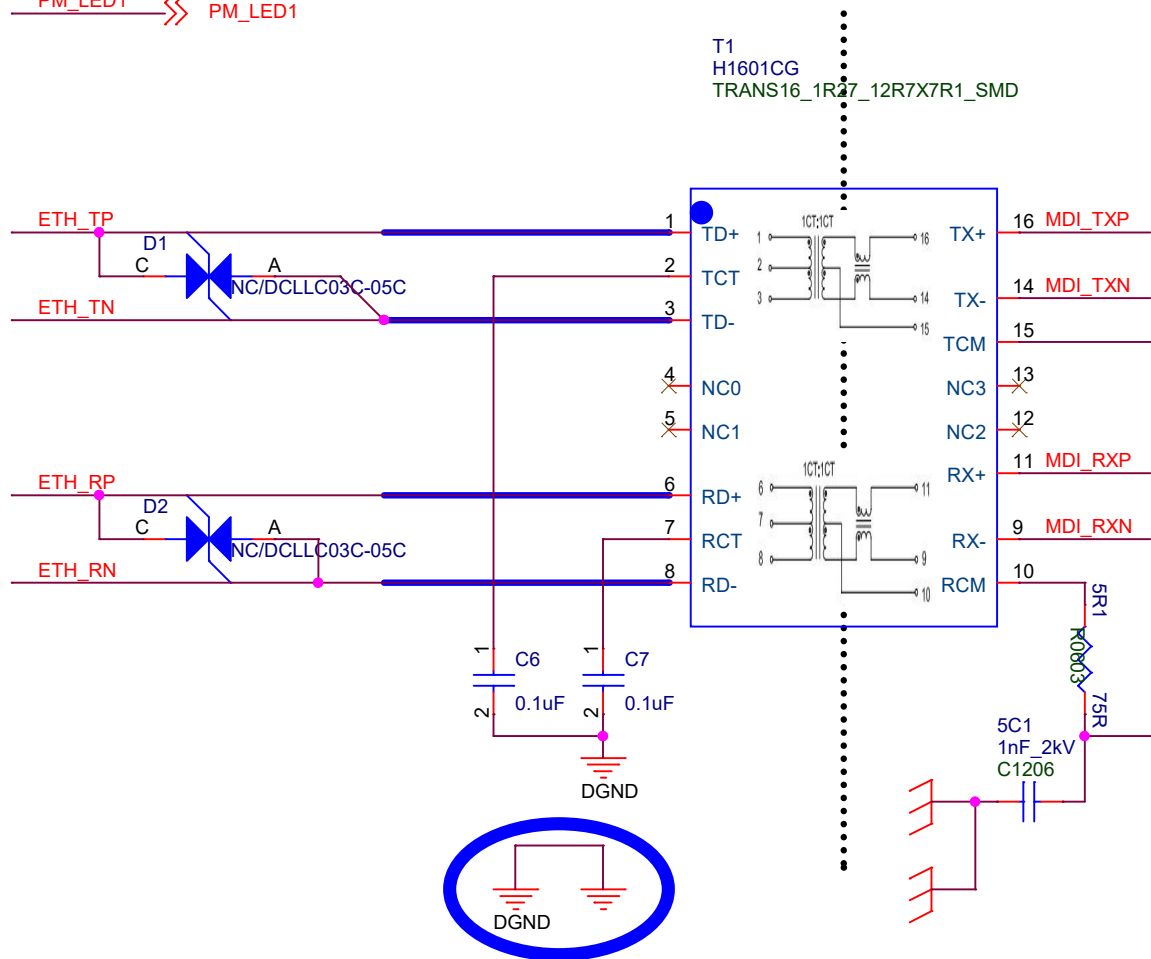
IR Receiver



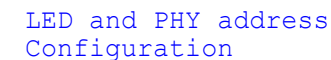
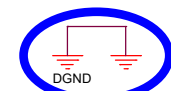
Geniatech			
Title	P01.KERNEL MODULE		
Size	Document Number	Rev	
B	RSOM20X-PLACODE	1.0	
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ETH_TP
ETH_TN
ETH_RP
ETH_RN

PM_LED0
PM_LED1



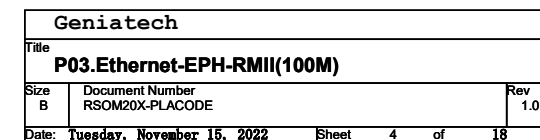
Geniatech		
Title		
P02.Ethernet-EPH(100M)		
Size	Document Number	Rev
A	RSOM20X-PLACODE	1.0
Date:	Tuesday, November 15, 2022	Sheet 3 of 18



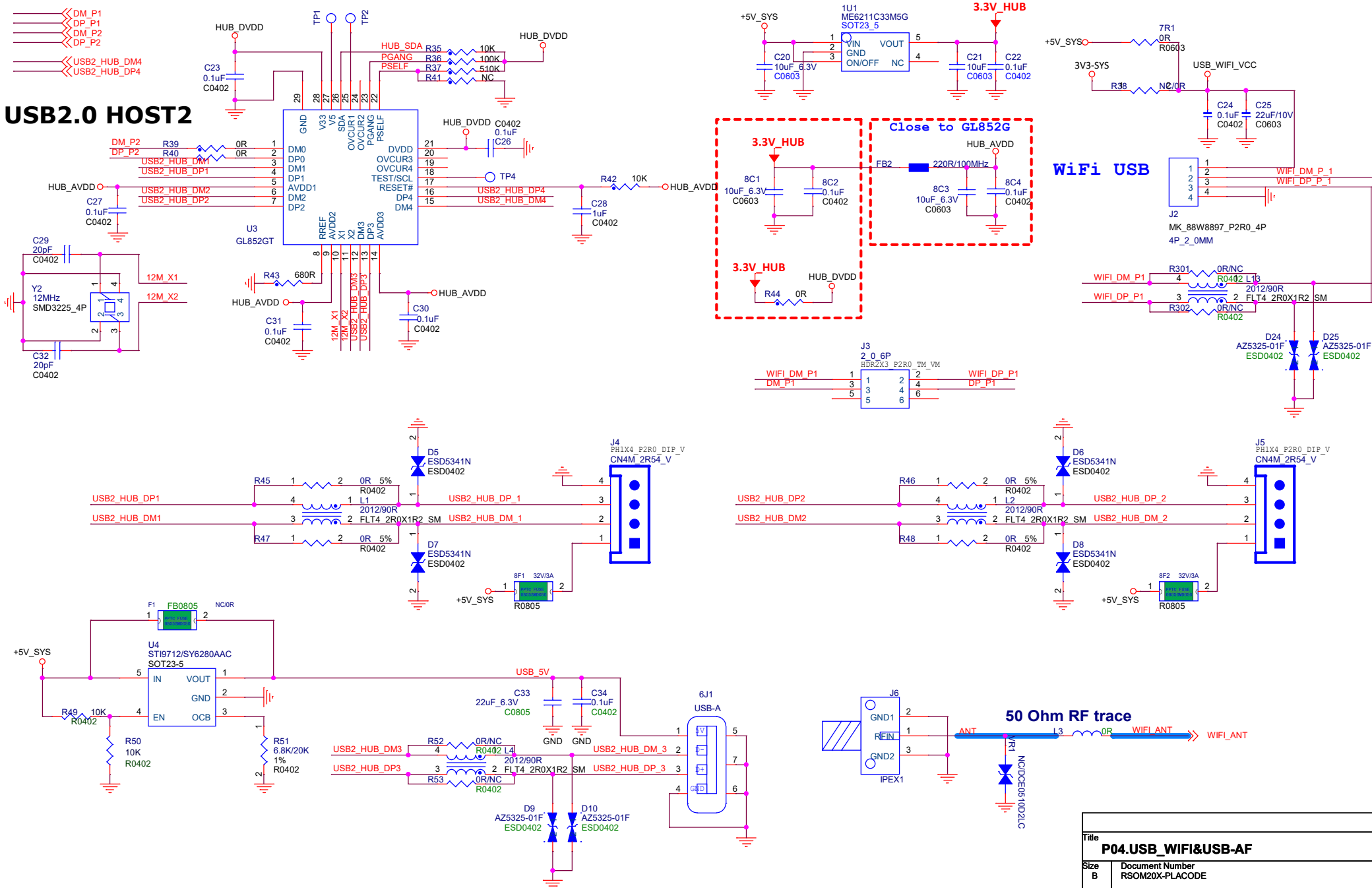
This schematic sets PHY address to 00001b.

1. Do not let these PHY address pins floating for the latched-in settings after the power is ready.

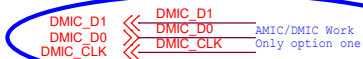
	Pull high	Pull down
COL/RMII	RMII mode	MII mode
CRS	LED mode2	LED mode1
RX_DV	Fiber mode	TP mode



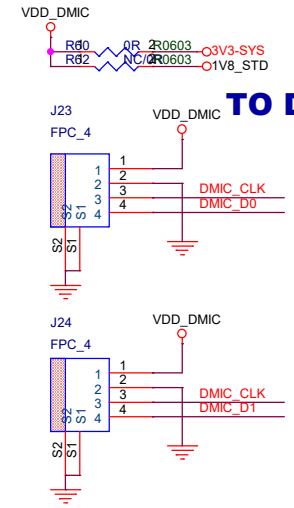
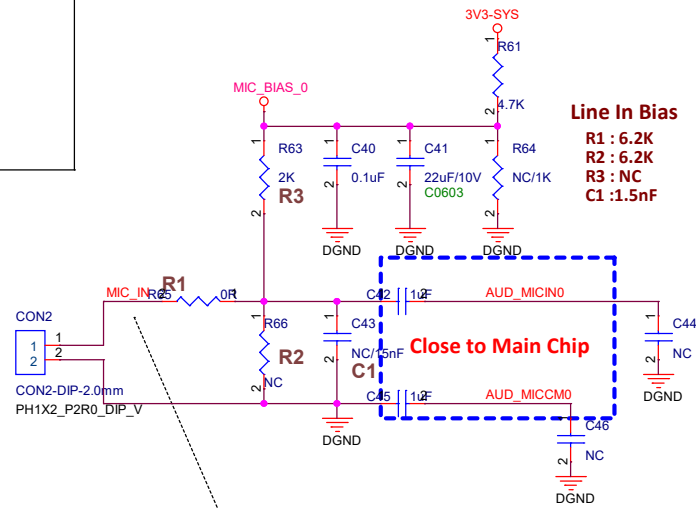
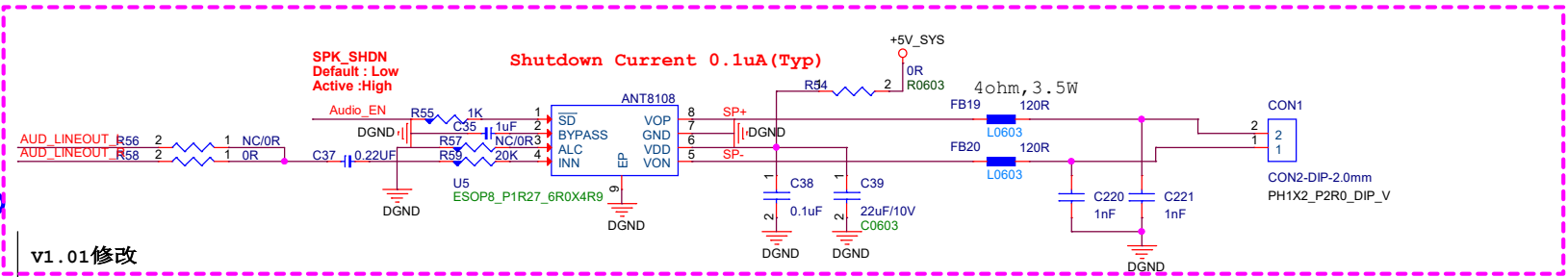
USB2.0 HOST2



Title				
P04.USB_WIFI&USB-AF				
Size B	Document Number R50M20X-PLACODE			Rev 1.0
Date:	Tuesday, November 15, 2022	Sheet	5 of	18



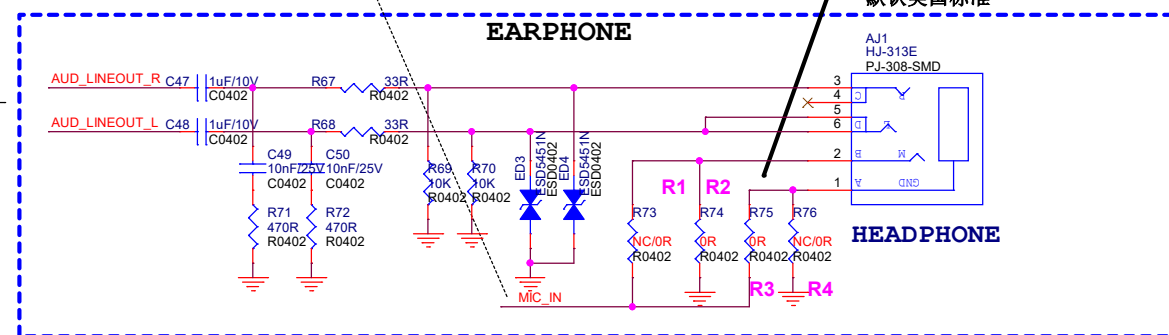
v1.01修改



TO DMIC

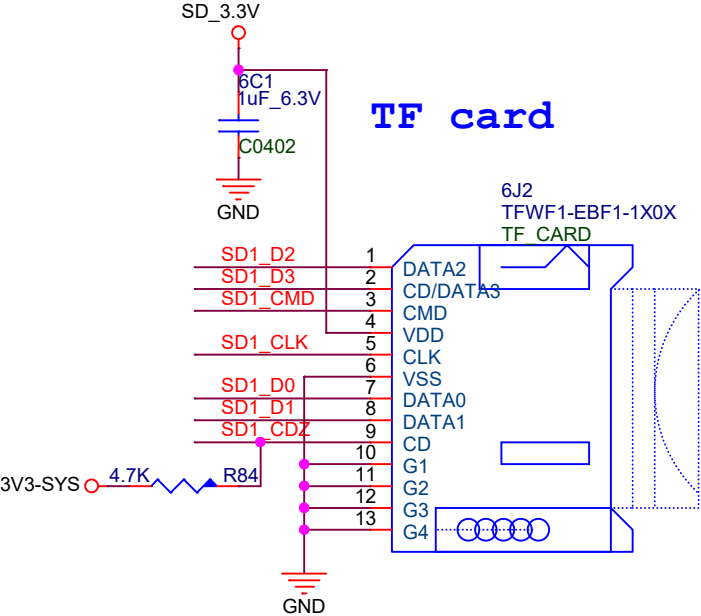
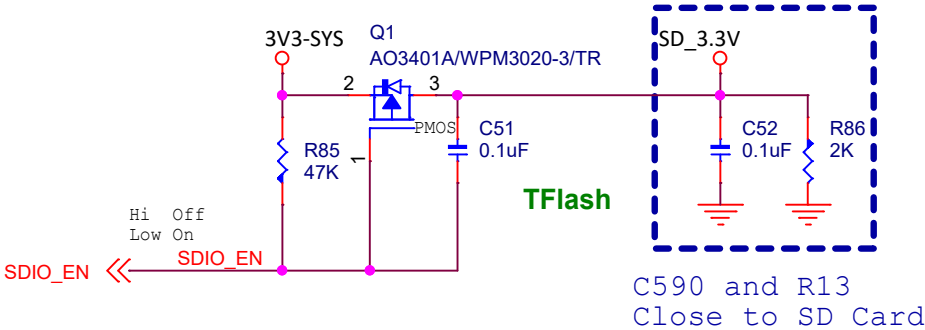
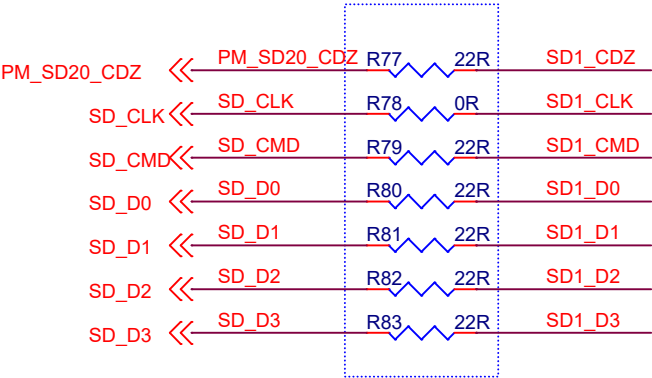
EARPHONE	R1	R2	R3	R4
欧洲标准	0R	NC	NC	0R
美国标准	NC	0R	0R	NC

默认美国标准

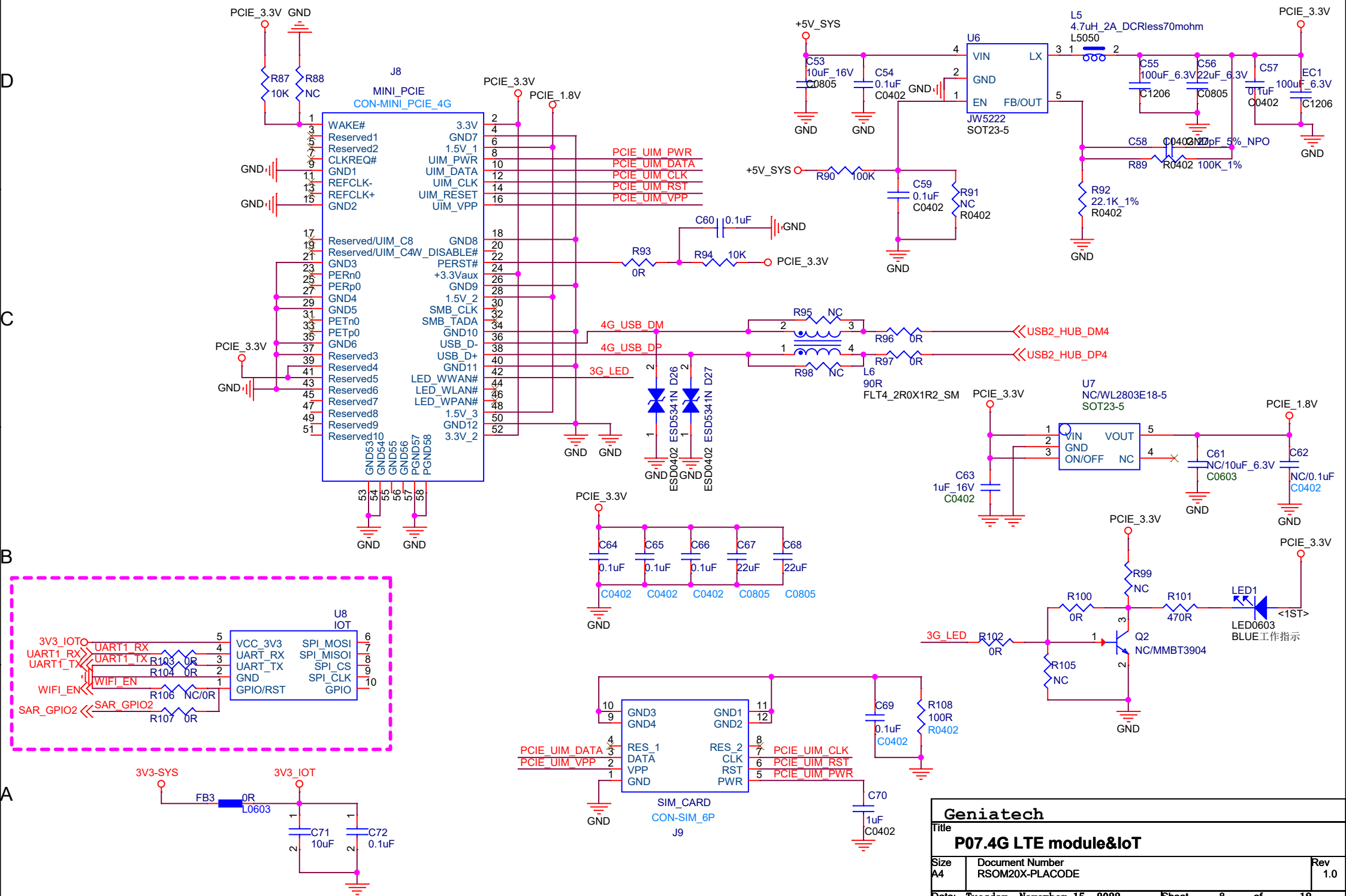


Geniatech		
Title P05. Audio		
Size B	Document Number RSOM20X-PLACODE	Rev 1.0
Date: Tuesday, November 15, 2022	Sheet 6	of 18

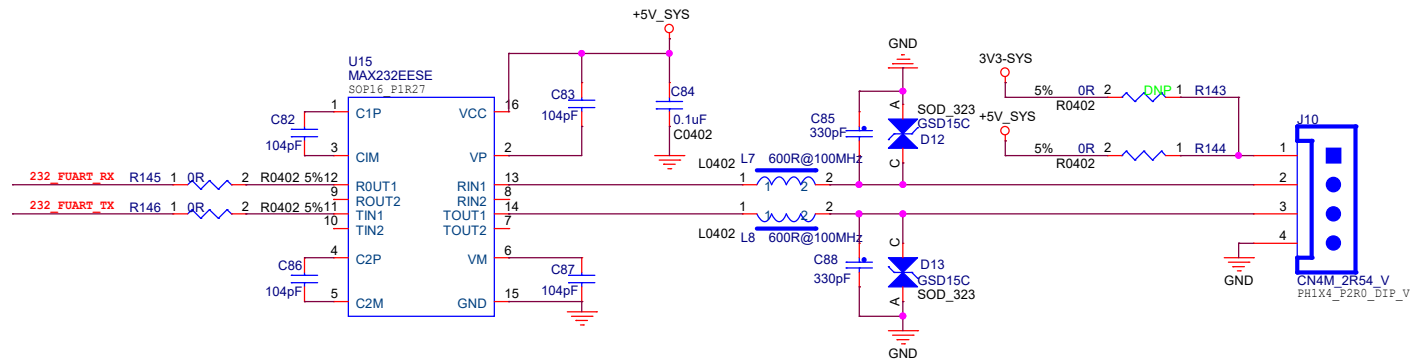
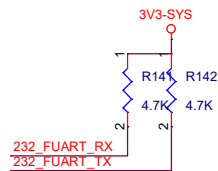
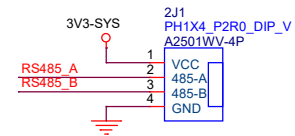
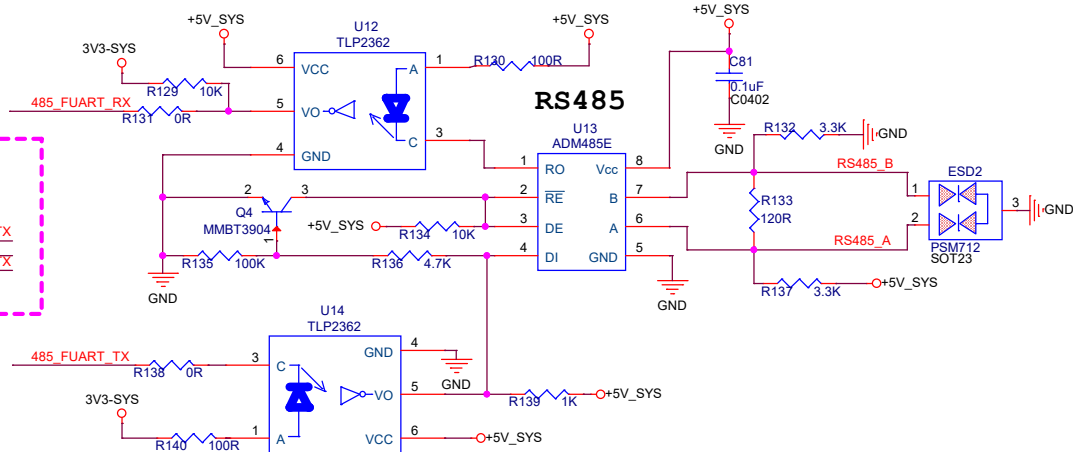
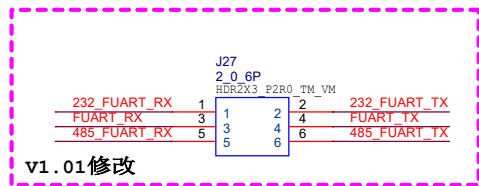
SDIO 2.0



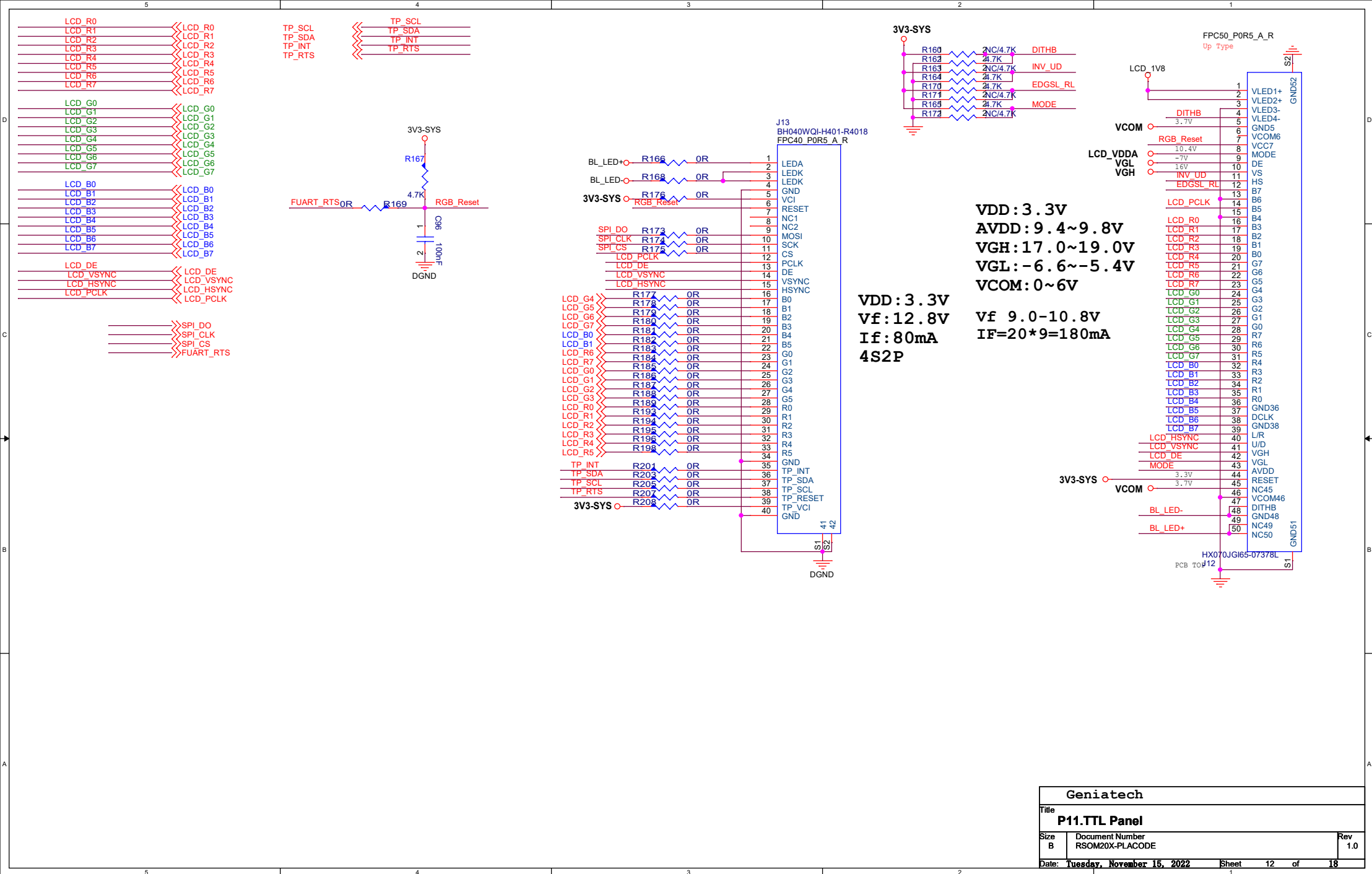
Geniatech		
Title		
P06.SDIO-TF CARD		
Size	Document Number	Rev
A	RSOM20X-PLACODE	1.0
Date: Tuesday, November 15, 2022		
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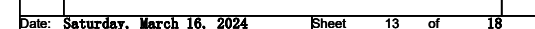


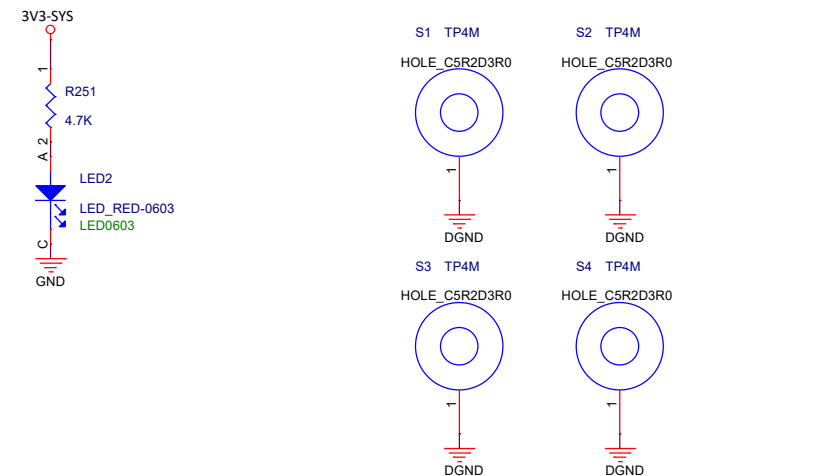
FUART_TX
 FUART_RX



Title		
P09.RS485/I2C/SPI		
Size	Document Number	Rev
B	RSOM20X-PLACODE	1.0
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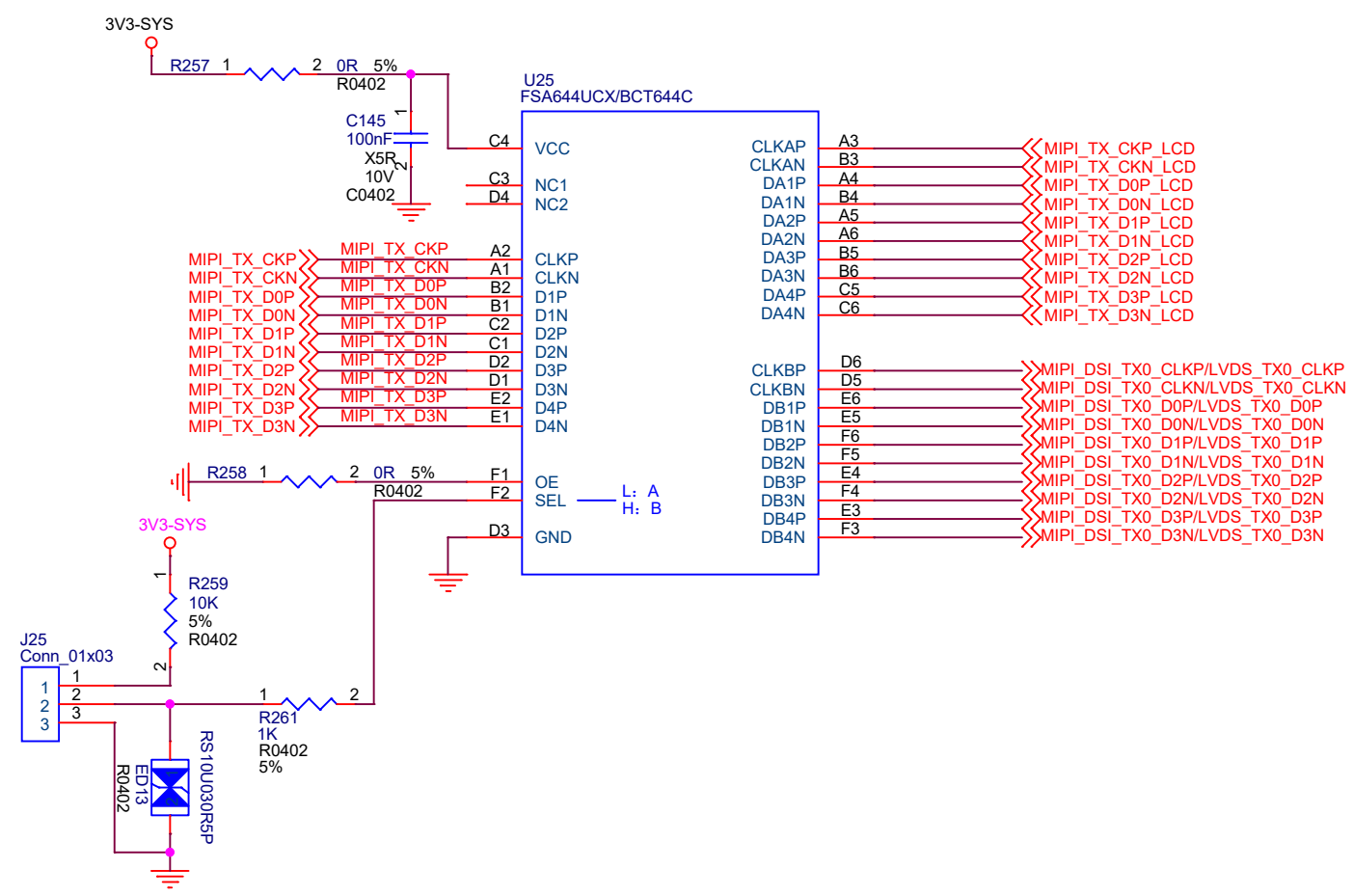


System Standby

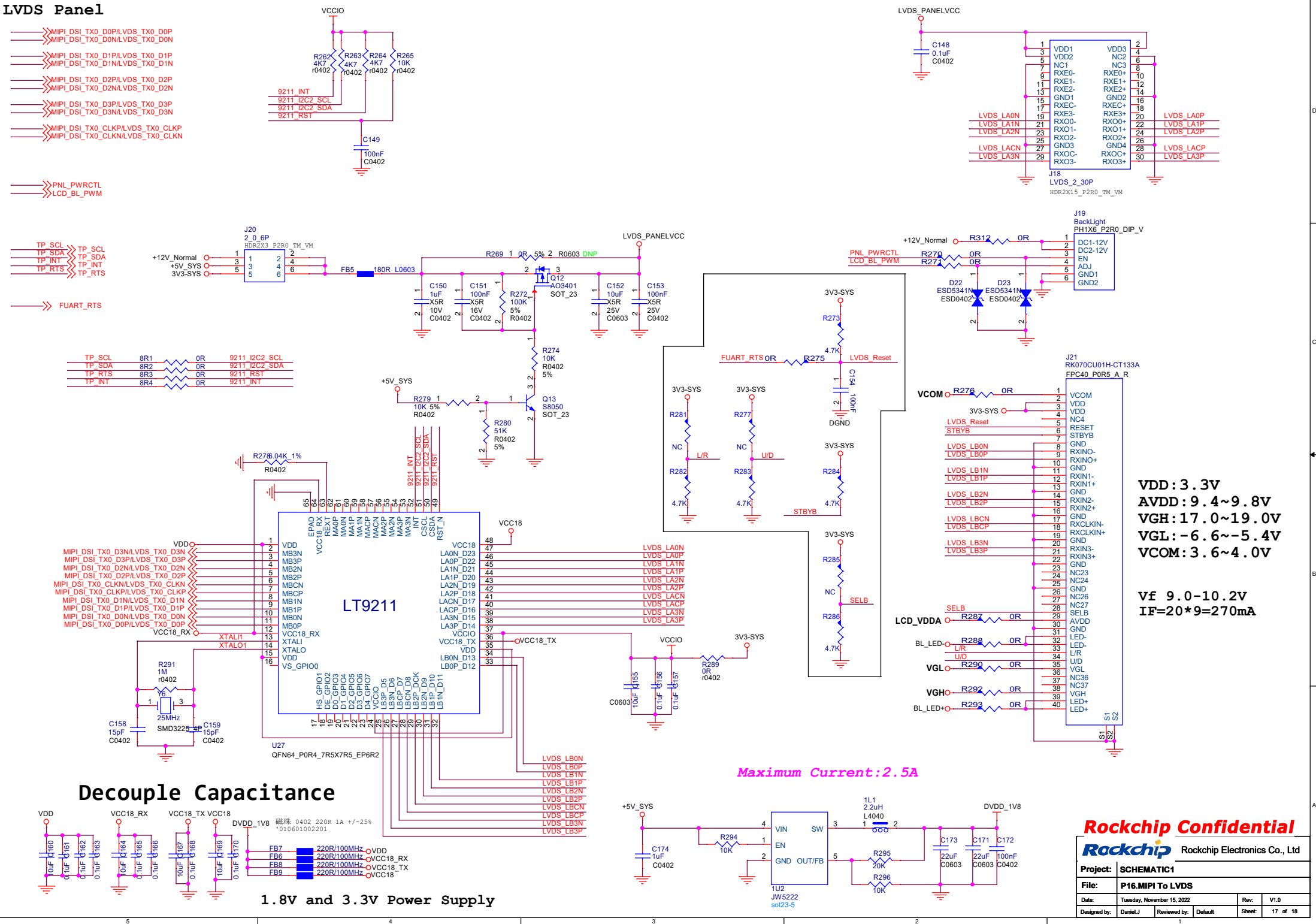
Title		
P13. Power		
Size B	Document Number RSOM20X-PLACODE	Rev 1.0
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REV	BY	DATE	DESCRIPTION
1.0	ZF	2021.02.02	First Release

Geniatech			
Title P14.Revision History			
Size A	Document Number RSOM20X-PLACODE		Rev 1.0
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LVDS Panel





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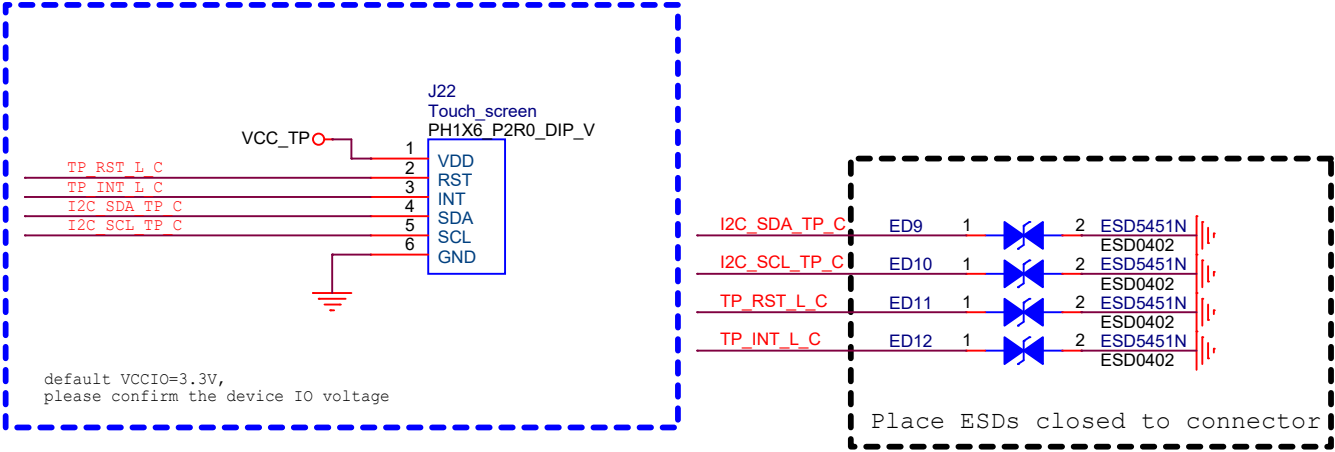
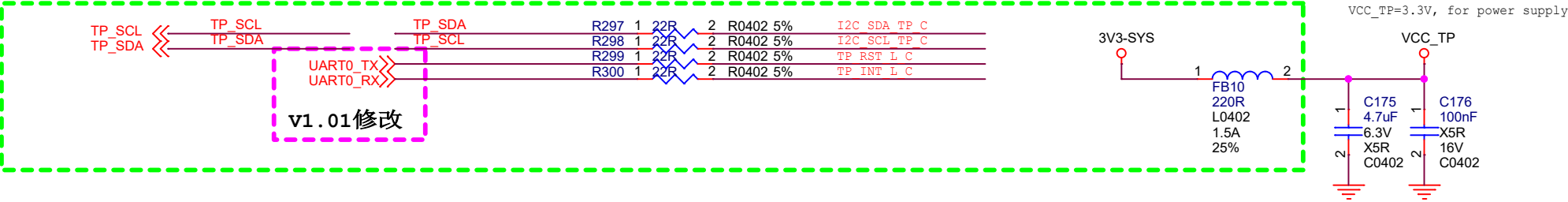


Rockchip Electronics Co., Ltd

Project: SCHEMATIC1

File:	P16.MIPI To LVDS		
Date:	Tuesday, November 15, 2022	Rev.	V1.0
Designed by:	Daniel.J	Reviewed by:	Default
		Sheet:	17 of 18

TP COF Connector



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Rockchip Electronics Co., Ltd

Project: SCHEMATIC1

File: P17.TP_Connector-COF

Date: Tuesday, November 15, 2022 Rev: V1.0

Designed by: Daniel.J Reviewed by: Default Sheet: 18 of 18